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REED-SOLOMON ENCODER/DECODER

APPENDICES TO
FINAL ENGINEERING REPORT

FEBRUARY 9, 1976

NADC
Not in DTIC
Tech. Info.

Prepared under Contract N62269-75-C-0503

DATA ITEM A003

for DTIC QUALITY INSPECTED 3

DISTRIBUTION STATEMENT A
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Department of the Navy
Naval Air Development Center

by

ITT Avionics Division
500 Washington Avenue
Nutley, N.J. 0110

85000276-1

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19970603 020

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

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20. ABSTRACT

ITT Avionics has built and successfully tested a RSED laboratory breadboard that was funded under contract N62269-75-C-0503 (Naval Air Development Center). A summary of the engineering tests is listed below.

Encoding Time	<150 microseconds
Round Trip Timing Detection	< 20 microseconds
Decode Time	Decode time is dependent on Errata. Refer to section 5 of report number D11801 for decode times.

APPENDIX A

RSED SPECIFICATIONS AND ENGINEERING DRAWINGS

Appendix A contains the specifications and engineering drawings generated under contract N62269-75-C-0503 (Reed-Solomon Encoder/Decoder).

<u>Specifications</u>	<u>Document Number</u>
Reed-Solomon Glossary of Notation	RS-3
Reed-Solomon Hardware	
Functional Specification	RS-9
Reed-Solomon Software Algorithms	RS-10
Requirements for RSED MicroProcessor Program Documentation	RS-14
Specification for RSED MicroProcessor (Breadboard Version)	RS-16

<u>*DRAWINGS</u>	<u>DWG. NUMBER</u>	<u>NUMBER OF SHEETS</u>
RS MCU/CPE	2618933	3
RS Memory	2618934	4
RS Encoder-Syndrome Generator	2618936	5
RS Data Steering	2618939	3
RSED Input/Output Buffer	2619235	4
RSED Control	2619236	3
RSED User Panel	2619237	13

*Drawings will be supplied as data item A008 under contract N62269-75-C-0503.

REED-SOLOMON GLOSSARY
OF NOTATION

SPECIFICATION NUMBER RS-3

REED-SOLOMON GLOSSARY OF NOTATION

$$C(x) = \text{Code Word Polynomial} = \sum_{i=0}^{30} C_i X^i$$

$$C_i = \text{Encoder Character in } i^{\text{th}} \text{ position}$$

$$C_{30} \rightarrow C_{16} = C_{30} \text{ First Transmitter Character}$$

$$C_{15} \rightarrow C_0 = \text{Parity Check Character}$$

$$r'(x) = \text{Received Code Word with Erasure indications}$$

$$r(x) = \text{Received Code Word (Same format as } c(x) \text{)} = \sum_{i=0}^{30} r_i X^i$$

$$S_x = \text{Syndrome Polynomial} = \sum_{k=1}^{16} S_k X^k$$

Define $S_0 \equiv 1$

$$S_k = k^{\text{th}} \text{ syndrome} = r(x) \big|_{x=\alpha^k}$$

$$\alpha = \text{Primitive Generator of GF (32)}$$

$\alpha^i \quad i=0 \rightarrow 30 =$ 31 Non-Zero Elements of GF (32)
 Represented by 5 bits.

B_{EL} = Erasure Location $B_{EL} = \alpha^l$

E_l = Erasure Location Numbers
 $l = 1 \rightarrow s$ if $r_m = \text{erasure}$, $E_e = m$

s = Number of erasures

$B_{EL}^{-1} = (\alpha^{31-EL})$ Roots of Erasure Location Polynomial, $B_{E_i} = \alpha^{E_i}$

$\sigma_E(x)$ = Erasures Location Polynomial

$$\sigma_E(x) = \sum_{i=0}^s \sigma_{E_i} x^i = \prod_{l=1}^s (1 + B_{EL} x)$$

$T'(x)$ = Forney's T Polynomial

$$T'(x) = (1 + S(x)) \sigma_E(x) = \sum_{m=0}^{\infty} T'_m x^m$$

T_j = Modified Syndromes

$$T_j = T'_{s+j}$$

$$T_j = \sum_{i=0}^s S_{s+j-i} \sigma_{E_i}$$

$$\sigma_e(x) = \text{Error Location Polynomial}$$

$$\sigma_e(x) = \sum_{i=0}^t \sigma_{ei} x^i$$

$$\beta_{ei}^{-1} = \text{Roots of Error Location Polynomial}$$

$$\beta_{ei} = \alpha^{ei}$$

$$e_{ii} = \text{Error Location Number } i = 1 - t$$

if $r_n = \text{error}$, then $e_i = n$

$$\sigma(x) = \text{Errata Location Polynomial}$$

$$\sigma(x) = \sum_{i=0}^{s+t} \sigma_i x^i$$

$$= \sigma_e(x) \sigma_E(x)$$

where

$$\sigma_i = \sum_{m+n=i} \sigma_{Em} \sigma_{En}$$

$$\tilde{Z}(x) = \text{Errata Evaluator Polynomial}$$

$$\tilde{Z}(x) = \sum_{i=0}^{s+t} \gamma_i x^i \equiv \sum_{i=0}^A \gamma_i x^i \quad A \leq s \text{ see note}$$

$$\tilde{Z}(x) = (1 + S(x)) \sigma(x) \text{ Mod } x^{s+t}$$

$$\gamma_i = \sum_{n+k=i} \sigma_n S_k \equiv \sum_{k+l+m=i} \sigma_{El} \sigma_{em} S_k$$

(Note: it is possible for $\gamma_i = 0$ for $i \geq A$, $A \leq s+t$)

$$\tilde{\tilde{Z}}(x) = \text{Modified Errata Evaluator Polynomial}$$

$$\tilde{\tilde{Z}}(x) = \sum_{i=s+t-A}^{s+t} \tilde{\gamma}_i x^i \equiv x^{s+t} \tilde{Z}\left(\frac{1}{x}\right)$$

$$\tilde{\gamma}_i = \gamma_{s+t-i}$$

B_i $=$

Inverse Roots of

 $\sigma_{E(X)}$

and

 $\sigma_{e(x)}$

$$i = (All B_{En}, B_{em})$$

 C_i' $=$

Errata Value for Location 1

$$C_i' = \frac{\sum (B_i)}{B_i \prod_{j \neq i} (\beta_i + \beta_j)}$$

REED-SOLOMON HARDWARE
FUNCTIONAL SPECIFICATION

SPECIFICATION NUMBER RS-9

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1.0

Galois Field - GF(32)

The field consists of 32 symbols represented by 5 binary bits. There are 31 non-zero symbols and 00000. Each field element is the anti-log of the field elements expressed as the integer powers of a base symbol called α . The anti-log representation will be called the code form of a symbol and the log representation will be called the power form of the symbol. The non-zero elements are shown in Table 1:

For example:

$$\log_{\alpha} (01000) = 1$$

$$\begin{array}{c} \circ \\ \circ \circ \end{array} 01000 = \alpha^1 = \alpha$$

$$\text{and anti-log}(1) = 01000$$

$$\log_{\alpha} (11111) = 15$$

$$\begin{array}{c} \circ \\ \circ \circ \end{array} 11111 = \alpha^{15}$$

$$\text{anti-log}(15) = 11111$$

$$\log_{\alpha} (10000) = 0$$

$$\begin{array}{c} \circ \\ \circ \circ \end{array} 10000 = \alpha^0$$

$$\text{By Definition } \alpha^{31} = \alpha^0 = 10000$$

1.1

Additions in GF(32) — $A + B = C$

Modulo 2 (XOR) bit by bit

$$\text{i.e. } A_4, A_3, A_2, A_1, A_0 = A \quad A_i \in (0, 1)$$

$$B_4, B_3, B_2, B_1, B_0 = B$$

$$C = C_4, C_3, C_2, C_1, C_0$$

where

$$C_i = A_i + B_i$$

1.2

Multiplication in GF (32) — $A (B) = C$

$$C = \text{Anti-log} \left((\log_{\alpha} A + \log_{\alpha} B) \text{ Mod } 31 \right)$$

$$\text{i.e. } \alpha^{15} (\alpha^{17}) = \alpha^{32 \text{ Mod } 31} = \alpha^1 = \alpha$$

Multiplication look up table can be provided in code form as a

1024 X 5 Table.

GALOIS FIELD TABLE

POWER FORM α^c	CODE FORM			CODE FORM			POWER FORM α^c
	BINARY	DEC	OCT	BINARY	DEC	OCT	
0	⁴³²¹⁰ 00001	1	1				
1	00010	2	2	00001	1	1	0
2	00100	4	4	00010	2	2	1
3	01000	8	10	00011	3	3	18
4	10000	16	20	00100	4	4	2
5	00101	5	5	00101	5	5	5
6	01010	10	12	00110	6	6	19
7	10100	20	24	00111	7	7	11
8	01101	13	15	01000	8	10	3
9	11010	26	32	01001	9	11	29
10	10001	17	21	01010	10	12	6
11	00111	7	7	01011	11	13	27
12	01110	14	16	01100	12	14	20
13	11100	28	34	01101	13	15	8
14	11101	29	35	01110	14	16	12
15	11111	31	37	01111	15	17	23
16	11011	27	33	10000	16	20	4
17	10011	19	23	10001	17	21	10
18	00011	3	3	10010	18	22	30
19	00110	6	6	10011	19	23	17
20	01100	12	14	10100	20	24	7
21	11000	24	30	10101	21	25	22
22	10101	21	25	10110	22	26	28
23	01111	15	17	10111	23	27	26
24	11110	30	36	11000	24	30	21
25	11001	25	31	11001	25	31	25
26	10111	23	27	11010	26	32	9
27	01011	11	13	11011	27	33	16
28	10110	22	26	11100	28	34	13
29	01001	9	11	11101	29	35	14
30	10010	18	22	11110	30	36	24
31	00001	1	1	11111	31	37	15

2.0 Encoder Specification

2.1 Input - 15 five bit data characters (in code form) denoted by m_0 through m_{14}

Format - (m_{14}, \dots, m_0)

2.2 Output - 31 five bit transmission characters, composed of the 15 original input characters and 16 computed (by Galois field arithmetic) characters denoted by $C_0 - C_{30}$

Format - (C_{30}, \dots, C_0)

The input characters are $C_{30} - C_{16}$ corresponding to $m_{14} - m_0$.

The computed characters are $C_{15} - C_0$ corresponding to $P_{15} - P_0$, therefore, the output format is $(m_{14}, \dots, m_0, P_{15}, \dots, P_0)$.

2.3 Process - P_i 's or C_i 's ($i = 15 - 0$) are computed according by the

following procedure: Fifteen constants (5 bits) are denoted by $h_0 - h_{14}$

(See Table 2). The recursion equation for C_j is given by

$$C_j = \sum_{i=0}^{14} h_i C_{j+15-i} \quad \text{for } j = 0 - 15$$

where $a \cdot b =$ Galois field multiplication

$a + b =$ Galois field addition

For Example, $P_{15} = C_{15}$ is

$$P_{15} = h_0 C_{30} + h_1 C_{29} + \cdot \cdot + h_{14} C_{16}$$

or

$$P_{15} = h_0 m_{14} + h_1 m_{13} + \cdot \cdot + h_{14} m_0$$

and

$$P_{14} = h_0 C_{29} + h_1 C_{28} + \cdot \cdot + h_{14} C_{15}$$

or

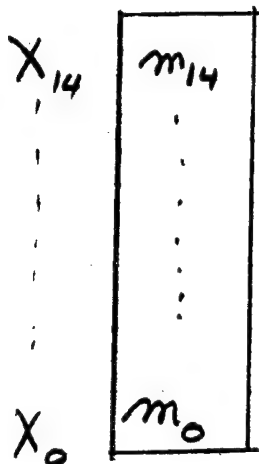
$$P_{14} = h_0 m_{13} + h_1 m_{12} + \cdot \cdot + h_{14} P_{15}$$

etc.

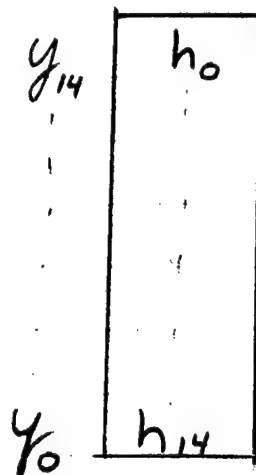
For additional clarity consider the input data $m_0 - m_{14}$ placed in an array $X_0 - X_{14}$, and the constants $h_0 - h_{14}$ placed in an array $Y_{14} - Y_0$ as shown.

ORIGINAL ARRAYS

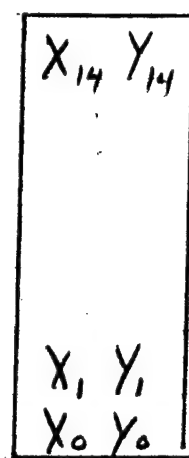
X ARRAY



Y ARRAY



Product
ARRAY

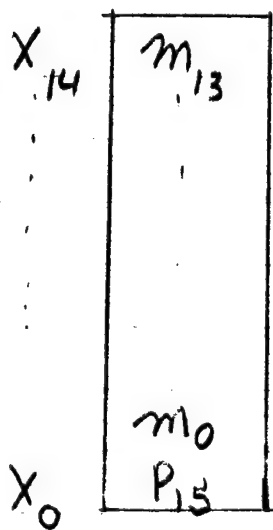


$$\oplus \sum x_i y_i = P_{15}$$

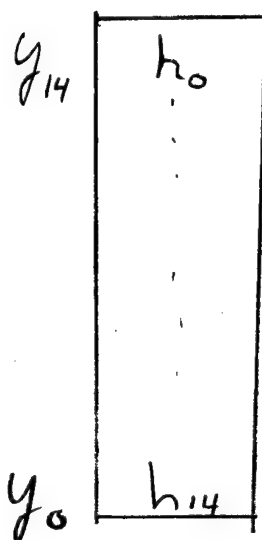
SECOND Computation For
 $x_i = x_{i-1}$ $x_0 = P_{15}$

P_{14}

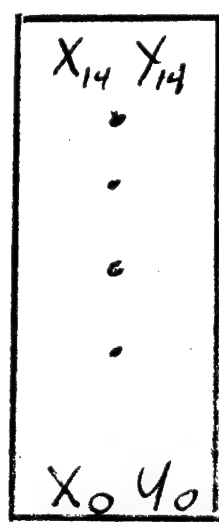
X ARRAY



Y ARRAY



Product
ARRAY



$$\sum x_i y_i = P_{14}$$

ETC. For $P_{13} - P_0$

Table 2./ h Constants

h	POWER FORM <i>2ⁱ</i> <i>i</i>	CODE WORD		
		OCTAL	BINARY	DECIMAL
		<i>0 1 2 3 4 5 6 7</i>		
h_0	19	6	00110	6
h_1	25	31	11001	25
h_2	3	10	01000	8
h_3	21	30	11000	24
h_4	6	12	01010	10
h_5	27	13	01011	11
h_6	9	32	11010	26
h_7	9	32	11010	26
h_8	16	33	11011	27
h_9	30	22	10010	18
h_{10}	0	1	00001	1
h_{11}	24	36	11110	30
h_{12}	22	25	10101	21
h_{13}	18	3	00011	3
h_{14}	23	17	01111	15
h_{15}	0	1	00001	1

3.0 Syndrome Generator

3.1 Input - 31 five bit characters (in code form) which are the received data with any arbitrary characters substituted for erasures.

Format - (r_{30}, \dots, r_0)

This represents the coefficient of the polynomial $r(x)$ in code form.

$$r(x) = \sum_{i=0}^{30} r_i X^i$$

3.2 Output - 16 five bit characters called Syndromes, $S_1 - S_{16}$ (in code form).

Format - (S_1, \dots, S_{16})

3.3 Process

By Definition

$$S_i = r(x) \big|_{x=\alpha^i}$$

OR

$$S_1 = r_{30} \alpha^{30} + r_{29} \alpha^{29} + \dots + r_1 \alpha + r_0$$

$$S_i = r_{30} (\alpha^i)^{30} + r_{29} (\alpha^i)^{29} + \dots + r_1 \alpha^i + r_0$$

$$S_{16} = r_{30} (\alpha^{16})^{30} + \dots + r_1 \alpha^{16} + r_0$$

Each S_i can be computed sequentially by factoring the equation.

$$S_i = r(x) \int_{x=\alpha^i} = ((r_{30} \alpha^i + r_{29}) \alpha^i) + r_{28} \alpha^i + \dots$$

Let $S_i(j)$ be the j^{th} partial product of S_i

Where

$$S_i(j) = \alpha^i S_i(j-1) + r_{30-j} \text{ for } j=0-30$$

and

$$S_i(-1) \equiv 0$$

Therefore:

$$S_i = S_i(30)$$

i.e.:

$$S_i(0) = \alpha^i \cdot 0 + r_{30} = r_{30}$$

$$S_i(1) = \alpha^i S_i(0) + r_{29} = \alpha^i r_{30} + r_{29}$$

$$S_i(29) = \alpha^i S_i(28) + r_1$$

$$S_i(30) = \alpha^i S_i(29) + r_0 = (\alpha^i)^2 S_i(28) + \alpha^i r_1 + r_0$$

Compute S_i by first encoding $r_{30} - r_{16}$ as in encoder get $P_{15} - P_0$.

$$\text{Compute } S'(X) = \sum_{i=0}^{15} s_i X^i$$

$$\text{Where } s_i = P_i + r_i \quad i = 0 - 15$$

and then compute

$$S_i = S'(X) \Big|_{X=\alpha^i} \quad \text{as in Option 1}$$

This requires only computing $S_i(15)$

$$\text{where } S_i(j) = \alpha^i S_i(j-1) + a_{15-j}$$

$$S_{i(15)} = (\alpha^i)^2 S_{i(14)} + \alpha^i s_1 + s_0$$

$\alpha^1 - \alpha^{16}$ are given in code form by power table \rightarrow code.

NOTE: Code 00000 = \emptyset has no power conversion

$$\emptyset(\alpha^i) = \emptyset_j \quad \emptyset + \alpha^i = \alpha^i$$

4.0 Erasure Location Process

4.1 Input - 31 six bit characters (code form)

Format - $(r_{30}, r_{29}, \dots, r_1, r_0)$

$r_i = \text{XXXXX0 data decision}$

$r_i = \text{XXXXX1 erasure decision}$

4.2 Output - 0 - 16 five bit numbers

Format (E_1, E_2, \dots, E_s)

4.3 Process - E_1 is the position number of an erasure.

If r_i, r_j, r_k are erasures

then $E_1 = i$

$E_2 = j$

$E_3 = k$

This leaves code 11111 to indicate end of list.

NOTE: If more than 16 erasures are detected word is not decoded and
FLAG is to be provided.

5.0 Error Correction Process

5.1 Input - 15 five bit character (code form) from the decoder.

Format - $(c'_{30}, \dots, c'_{16})$

These are data correction characters where $c'_i = \phi$ if character correct.

5.2 Output - 15 five bit corrected data characters (code form)

Format - (d_{30}, \dots, d_{16})

5.3 Process - The d_i 's are computed by $d_i = r_i + c'_i$

where r_j ($j = 30$ to 16) are the received data characters

NOTE: See Radio Relay Process if Flag for radio relay is set.

6.0 Radio Relay Process

6.1 Function

At start of time slot, the communication processor will flag the signal processor that the incoming message is to be relayed. This must set an indicator.

6.2 Input

45 five bit corrected data characters (code form)

Format: (d_{14}, \dots, d_0) (d_{14}, \dots, d_0) (d_{14}, \dots, d_0)
 First Word Word 2 Word 3

6.3 Output

One of the bits of the three words (TBD) is set to 1 and the words are sent to the encoder.

7.0 Maximum Likelihood RTT Decoder

7.1 Input - 16 six bit characters (code form)

Format: - $(r_{15}, r_{14}, \dots, r_1, r_0)$

$r_i = \text{XXXXX}(0)$ data decision

$r_i = \text{XXXXX}(1)$ erasure

7.2 Output - 1 bit - Yes or No

i.e., Match or No Match

7.3 Process - Stored Reference - $(A_{15}, A_{14}, \dots, A_1, A_0)$

16 five bit number

Compare r_i with A_i , Result = $B_{(i)}$ a number

If r_i , an erasure, $B_{(i)} = 1$

If r_i , a data decision

Compare first 5 bits of r_i with A_i

If $r_i = A_i$, $B_{(i)} = 2$

If $r_i \neq A_i$, $B_{(i)} = 0$

Compute $\sum_{i=0}^{15} B_{(i)}$ and compare to threshold $T = 20$

If $\sum_{i=0}^{15} B_{(i)} \geq 20$; output = Match

If $\sum_{i=0}^{15} B_{(i)} < 20$; output = Mismatch

8.0 Encoding of $(16, 4)$ code.

8.1 Input

Four 5 bit data characters

Format

(m_3, \dots, m_0)

8.2 Output

Sixteen 5 bit transmission characters.

$(c_{15}, \dots, c_8, c_7, \dots, c_0)$

which are:

$(m_3, \dots, m_0, P_{15}, \dots, P_4)$

8.3 Process

Encode m_0, m_1, m_2, m_3 , as a 15 character word by generating

$(m_{14}, \dots, m_4, \dots, m_0)$

where $m_4, \dots, m_{14} \equiv \emptyset$

Compute $P_4 - P_{15}$, the first twelve parity check characters as in encoder specification.

9.0 Decoding 16, 4 code word.

9.1 Input

Sixteen 6 bit characters from signal processor denoted by, r_i'
with erasures = XXXXX1

$$(r_{15}', \dots, r_0') \quad 1)$$

Convert to 31 character format

$$(r_{30}', \dots, r_{15}', \dots, r_0') \quad 2)$$

$$\begin{aligned} \text{where } r_i &= r_{i-4}' & i &= 4, \dots, 19 \\ r_i &= \phi & i &= 20 - 31 \\ r_i &= \text{erasure} & i &= 0 - 3 \end{aligned}$$

9.2 Output

9.2.1 Erasure Locations: (E_1, \dots, E_s) as in Erasure Location

Process for 2)

$$\text{i.e., } E_i = i - 1 \quad i = 1-8, \text{ and others.}$$

9.2.2 Syndromes: $S_1 - S_{16}$ as in Syndrome Generator for 2).

9.3 Error Correction: Same as (31, 15) word using 2). Output only

$$d_{16} - d_{19}.$$

9.4 Relay Mode - Encode $d_{16} - d_{19}$ as $m_0 - m_3$ in encoder.

APPENDIX A

REED-SOLOMON SOFTWARE ALGORITHM

SPECIFICATION NUMBER RS-10

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1.0 Erasure Polynomial Generator (APGEN)

1.1 Input

$E_1, 1 = 1, \dots, s$ Erasure Location Numbers

(If $r_K \equiv$ erasure, $E_1 = K, \forall K$)

1.2 Output: $s+1$ coef. $\sigma_{E_i} \quad i = 0, \dots, s$

$\sigma_{E_0} \equiv 1$, Coef. of Erasure Polynomial

$$\begin{aligned}\sigma_E(X) &= \sum_{i=0}^s \sigma_{E_i} X^i = \prod_{l=1}^s (1 + \alpha^{E_l} X) \\ &= \prod_{l=1}^s (1 + \beta_{E_l} X) ;\end{aligned}$$

where $\beta_{E_1} =$ Inverse roots of $\sigma_E(X) = \alpha^{E_1}$

1.3 Process:

In general

$$\begin{aligned}\sigma_{E_0} &= 1 \\ \sigma_{E_1} &= \sum_{\forall E_1} \beta_{E_1} \\ \sigma_{E_2} &= \sum_{\substack{\forall E_1, E_2, \\ i \neq j}} \beta_{E_1} \beta_{E_2} \\ \sigma_{E_{s-1}} &= \sum_{\forall E_j} \left(\frac{\alpha}{\prod_{i=1}^{s-1} \beta_{E_i}} \right)\end{aligned}$$

Simplify notation $\beta_i \equiv \beta_{E_i}$

can compute σ_{E_i} by the following iterative process.

Define $A_i(s) = \sigma_{E_i}$ $i = 0, \dots, s$

where $A_i(j)$ = the j^{th} value of A_i iterate till $j = s$

$$A_i(j) = A_{i-1}(j-1) \beta_j + A_i(j-1) ; i < j$$

$$A_i(i) = A_{i-1}(i-1) \beta_i + 0 ; j=i$$

$$A_i(j) \equiv 0 ; i > j$$

$$A_0(j) = A_0(j-1) \equiv 1 ; \forall j$$

First iteration $j = 1$

$$A_0(1) = 1$$

$$A_1(1) = \beta_1$$

$j = 2$

$$A_0(2) = 1$$

$$A_1(2) = A_0(1) \beta_2 + A_1(1) = \beta_2 + \beta_1$$

$$A_2(2) = A_1(1) \beta_2 + A_2(1) = \beta_1 \beta_2 \text{ etc.}$$

2.0 Modified Syndromes T_j MSYNG

2.1 Inputs

$$S_i \quad i = 1, \dots, 16$$

$$\sigma_{E_i} \quad i = 0, \dots, s \quad \sigma_{E_0} \equiv 1$$

Simplify notation $\sigma_{E_i} = \sigma_i$

2.2 Output

$$T_j \quad j = 1, \dots, (16-s)$$

2.3 Process:

$$T_j = \sum_{i=0}^s S_{s+j-i} \sigma_i$$

i.e., $T_1 = S_{s+1} + \sigma_1 S_s + \sigma_2 S_{s-1} + \dots + \sigma_s S_1$

$$T_2 = S_{s+2} + \sigma_1 S_{s+1} + \sigma_2 S_s + \dots + \sigma_s S_2$$

$$T_{16-s} = S_{16} + \sigma_1 S_{15} + \sigma_2 S_{14} + \dots + \sigma_s S_{16-s}$$

Array: $\sigma \quad y(1) \quad y(2)$

X_0	σ_0	$Y_0(1)$	S_{s+1}	$Y_0(2)$	S_{s+2}	Push down Stack
X_1	σ_1	$Y_1(1)$	S_s	$Y_1(2)$	S_{s+1}	
X_2	σ_2	$Y_2(1)$				
\vdots	\vdots	\vdots	\vdots	\vdots		
\vdots	\vdots	\vdots	\vdots	\vdots		
X_s	σ_s	$Y_s(1)$	S_1	$Y_s(2)$	S_2	

$$T_1 = \sum_{i=0}^s X_i Y_i(1)$$

$$T_2 = \sum_{i=0}^s X_i Y_i(2)$$

2.4

Modified Syndromes Berlekamp Notation

In general case, define T_j^1 as the coefficient of X^j in the equation.

$$(1 + S(X)) \sigma_E(X) = T^1(X) = \sum_{j=0}^{s+16} T_j^1 X^j$$

$$S(X) = \sum_{i=1}^{16} S_i X^i$$

$$\sigma_E(X) = \sum_{i=0}^s \sigma_{E_i} X^i, \quad s = \# \text{ of erasures}$$

Then T_i 's on previous page are $T_i = T_{s+i}^1$

3.0

Error Location Polynomial

 $\sigma_e(X)$

EPGEN

3.1

Input

Modified Syndromes T_j (5 bits)

$$j = 1, \dots, (16-s)$$

Where s = number of Erasures

If $s = 0$; $T_j = S_j$, $j = 1, \dots, 16$

3.2 Output

$t + 1$ Coefficient of Error Location

Polynomial (5 bits) σ_{e_i} $i = 0, \dots, t$

t = number of errors

where $\sigma_{e_0} \equiv 1$

3.3 Process - Simplify notation $\sigma_{e_i} = \sigma_i$

3.3.1 Option 1 Berlekamp Algorithm

This is iterative Process $K = 0, \dots, (16-s)$

Define values of K^{th} iteration (depends only on $K-1$)

$$\sigma^{(K)}(x) = \sum_{i=0}^n \sigma_i^{(K)} x^i = \text{Error Loc. Polynomial}$$

$\sigma_i^{(K)}$ GF (32) element

$$\tau^{(K)}(x) = \sum_{i=0}^m \tau_i^{(K)}(x)^i = \text{Tau Polynomial}$$

$\tau_i^{(K)} = \text{GF}(32) \text{ element}$

$B(K)$ = Computation Number (Decimal)

$D(K)$ = Computation Number (Decimal)

$\Delta^{(K)}$ = Coefficient index - GF(32) element

0th Iteration

Define $\sigma^{(0)}(x) \equiv 1$

$\tau^{(0)}(x) \equiv 1$

$$D(o) \equiv 0$$

$$B(o) \equiv 0$$

In general

$$\Delta^{(K)} = \sum_{m+n=K+1} T_m \sigma_n^{(K)} = T_{K+1} \sigma_o^{(K)} + T_K \sigma_1^{(K)} + \dots + T_o \sigma_{K+1}^{(K)}$$

Define $\tau \equiv 1$

i.e., $\Delta^{(K)} =$ Coefficient of X^{K+1} in $(1+T(X)) \sigma^{(K)}(X)$

$$T(X) = 1 + \sum_{i=1}^{16-A} T_i X^i$$

$$\sigma^{(K+1)}(X) = \sigma^{(K)}(X) + \Delta^{(K)} \tau^{(K)}(X) X$$

$$\text{or } \sigma_i^{(K+1)} = \sigma_i^{(K)} + \Delta^{(K)} \tau_{i-1}^{(K)} \quad \forall i \leq \text{max degree} \\ (\sigma^K(X), \tau^{(K)}(X))$$

The value of $D(K+1)$, $B(K+1)$ and $\tau^{(K+1)}(X)$ are computed from the two equations A and B by the rules below.

A: $D(K+1) = D(K)$

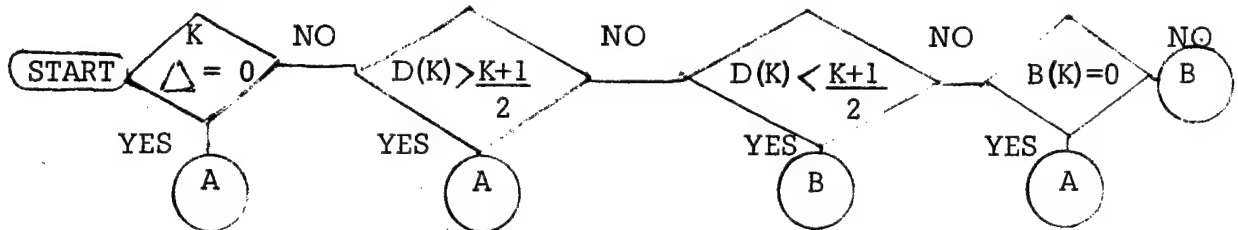
$$B(K+1) = B(K)$$

$$\tau^{(K+1)}(X) = \tau^K(X) \text{ or } \tau_i^{(K+1)} = \tau_i^{(K)}$$

B: $D(K+1) = K+1-D(K)$ (decimal arithmetic)

$B(K+1) = 1-B(K)$ (decimal arithmetic)

$$\tau_i^{(K+1)} = \sigma_i^{(K)} \frac{1}{\Delta^{(K)}}$$



Continue until $K = 16-s$ and $\bar{\sigma}_e(X) = \bar{\sigma}^{(16-s)}(X)$.

3.3.2 Option 2 Shu Lin Algorithm (Berlekamp Modified)

Iterative process with reliance on earlier results,

u^{th} iteration depends on $u-1, u-2$, etc..

Define values of u^{th} iteration, $u = -1, \dots, (16-s)$.

$$\sigma^{(u)}(X) = \sum_{i=0}^n \sigma_i^{(u)} X^i = \text{error location polynomial}$$

d_u = Coef Index GF32 element $\equiv \Delta^{(K)}$

l_u = Computation number.(decimal)

$u - l_u$ = Computation Number. (decimal)

th
-1 iteration

th
0 iteration

Define:

$$\sigma^{(-1)}(X) = 1$$

$$\sigma^{(0)}(X) = 1$$

$$d_{-1} = 1$$

$$d_0 = T$$

$$l_{-1} = 0$$

$$l_0 = 0$$

$$\sigma^{(16-s)}(X) \equiv \sigma_e(X)$$

In general, compute u+1st row according to value of

d_u by (A') or (B') where:

$$d_u = \sum_{\forall m+n=u+1} T_{m \ n} \sigma^{(u)} = T_{u+1 \ 0} \sigma^{(u)}_0 + \dots + T_{0 \ u+1} \sigma^{(u)}_{u+1}$$

$$T_{0 \ 0} = 1$$

A': If $d_u = 0$ (00000)

$$\sigma^{u+1}(X) = \sigma^{(u)}(X)$$

$$l_{u+1} = l_u$$

B': If $d_u \neq 0$ find previous row, ρ , such that $d_\rho \neq 0$

and $(\rho - l_\rho) \geq (\tau - l_\tau) \quad \forall \tau < u$

(or $(\rho - l_\rho)$ is maximum)

$$\text{Then } \sigma^{(u+1)}(X) = \sigma^{(u)}(X) + d_u d_\rho^{-1} X^{u-\rho} \sigma^{(\rho)}(X)$$

$$\text{or } \sigma_i^{(u+1)} = \sigma_i^{(u)} + d_u d_\rho^{-1} \sigma_{i-(u-\rho)}^{(\rho)}$$

$$l_{u+1} = \text{Max} [l_u, l_{\rho+u-\rho}]$$

4.0 Inverse Roots of $\sigma_e(X) = \beta_{e_i} \quad i = 1, \dots, t \quad \text{EPVAL}$

4.1 Input

$t + 1$ coefficients of $\sigma_e(X) = \sigma_{e_i} \quad i = 0, \dots, t$

$$\sigma_{e_0} \equiv 1$$

4.2 Output

t distinct inverse roots of $\sigma_e(X)$

If there are less than t roots then decoding is in error and an error will be flagged.

$$\beta_{e_i} \quad i = 1, \dots, t$$

$$\beta_{e_i} = \alpha^{e_i} \quad \text{error in location} \quad r_{e_i}$$

4.3 Process

Compute $\sigma_e(X) \quad X = \alpha^j$

If $\sigma_e(\alpha^j) \equiv \phi, (00000)$

Then $\beta_{e_i}^{-1} = \alpha^j$ and $\beta_{e_i} = \alpha^{31-j}$

$$\sigma_e(\alpha^j) = \sum_{n=0}^t \sigma_{e_n} (\alpha^j)^n$$

can be computed sequentially as S_K

$$\sigma_e(\alpha^j) = ((\sigma_{e_t} \alpha^j + \sigma_{e_{t-1}}) \alpha^j + \sigma_{e_{t-2}}) \alpha^j + \dots$$

5.0 Errata Evaluator Polynomial $\tilde{Z}(X)$ RPGEN

5.1 Input

Sixteen Syndromes $S_1 \dots S_{16}$ S_i

s = coefficients of the Erasure Polynomial $\sigma_{E_0} \dots \sigma_{E_s} \sigma_{E_i}$

t = coefficients of the Error Location Polynomial $\sigma_{e_0} \dots \sigma_{e_t} \sigma_{e_i}$

5.2 Output

Coefficients of $\tilde{\gamma}_i$ (a variable number)

5.3 Process

$$Z(X) = (1 + S(X)) \sigma_E(X) \sigma_e(X) = \sum_{i=0}^{s+t} \gamma_i X^i$$

$$= (1 + S(X)) \sigma_E(X) \sigma_e(X) \bmod Z^{s+t+1}$$

Only the coefficients of $X^0, X^1, X^2, \dots, X^{s+t}$ are required

where s = # of erasures = the degree of $\sigma_E(X)$

t = # of errors = the degree of $\sigma_e(X)$

$$\therefore \gamma_i = \sum \sigma_{E_l} \sigma_{e_m} S_K$$

$$\gamma_0 \equiv 1, \sigma_{e_0} \equiv 1, \sigma_{E_0} \equiv 1$$

for all $K + l + m = i$

Note:

It is possible for $\gamma_i = 0$ for $i > A$, $A < s + t$

$$\therefore Z(X) = \sum_{i=0}^A \gamma_i X^i \quad A \leq s+t$$

$$\text{Now } \tilde{Z}(X) = X^{s+t} Z(1/X) = \sum_{i=s+t-A}^{s+t} \tilde{\gamma}_i X^i$$

$$\text{where } \tilde{\gamma}_i = \gamma_{s+t-i} \quad i = (s+t-A), \dots, (s+t)$$

6.0 Errata Value Calculator (RPVAL)

6.1 Input

sent values β_{E_i}, β_{e_i}

all inverse roots of $\sigma_E(X)$ and $\sigma_e(X)$

where $\beta_{E_i} = \alpha^{E_i}$
 $\beta_{e_i} = \alpha^{e_i}$ } Denotes errata in received
character r_{E_i} and r_{e_i}

Let β_{E_i} and β_{e_i} be denoted by β_i

where $i = E_i$ or e_i

Then $\beta_i = \alpha^i$ $i = (E_i, e_i) = \text{errata location}$

6.2 Output

C'_i = Errata value for location i

$i = 16, \dots, 30$ (all data locations)

6.3 Process

$C'_i = 0$ (00000) $\forall i \neq E_i$ or e_i

$C'_i = \frac{\tilde{Z}(\beta_i)}{\beta_i \prod_{i \neq j} (\beta_i + \beta_j)}$ $\forall i, j = E_i$ or e_i

$$\tilde{Z}(\beta_i) = \sum_{n=s+t-A}^{s+t} \tilde{\gamma}_n(\beta_i)^n$$

can be computed sequentially as in S_k computation

$$\tilde{Z}(\beta_i) = ((\tilde{\gamma}_{s+t}\beta_i + \tilde{\gamma}_{s+t-1})\beta_i + \tilde{\gamma}_{s+t-2})\beta_i \dots$$

Option 2:

$$C'_i = \frac{Z(\beta_i)^{-1}}{\prod_{i \neq j} (1 + \beta_j \beta_i^{-1})}$$

$$\text{where } \beta_i^{-1} = \beta_{e_i}^{-1} = \alpha^{31-e_i}$$

$$\beta_i^{-1} = \beta_{E_i}^{-1} = \alpha^{31-E_i}$$

REQUIREMENTS FOR RSED MICROPROCESSOR

PROGRAM DOCUMENTATION

SPECIFICATION NUMBER RS-14

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1.0 INTRODUCTION

1.1 PURPOSE

This specification establishes a set of requirements for the preparation of digital microprocessor program technical documentation for the RSED. The specification is a modification of NAVORD WS-8506 and has similar technical content.

1.2 SCOPE

The microprocessor program documentation consists of the following items:

1.2.1 MICROPROCESSOR PROGRAM FUNCTIONAL SPECIFICATION (MPFS)

The MPFS describes the functional requirements for the microprocessor program of the RSED. The MPFS describes the function in terms of operational, functional, and mathematical language.

1.2.2 MICROPROCESSOR PROGRAM DESIGN SPECIFICATION (MPDS)

The MPDS contains the design details for the microprocessor program. The MPDS is written in programming terminology and translates the requirements of the Functional Specification into technical programming detail. It is specifically oriented to programming logic and programmer's language. A detailed description of all data items according to their type, purpose, size, range of values and structure is provided together with appropriate cross referencing.

The MPDS presents the results of the programming efforts and provides the verification that the program fulfills the original requirements.

1.2.3 MICROPROCESSOR PROGRAM PACKAGE (MPP)

The MPP consists of the physical microprocessor program in the form of paper tape/punched cards and program listings.

2.0 APPLICABLE DOCUMENTS

American National Standards Institute Inc. X3.5-1970 Flowchart Symbols and Their Usage for Information Processing.

3.0 MICROPROCESSOR PROGRAM DOCUMENTATION

Microprocessor program documentation for the RSED shall be as specified in Sections 4 and 5.

3.1 SYMBOLS FOR FLOWCHARTS AND TEXT

Flowchart symbols and logic symbols for flowcharts and text shall be as specified in the latest American National Standards Institute Document X3.5-1970.

3.2 DOCUMENT PREPARATION

All documents shall be prepared in accordance with the requirements specified in the following paragraphs.

3.2.1 NOMENCLATURE

References to the nomenclature shall be made as follows:

1. Acronyms, elisions, and nicknames shall be spelled with all capital letters, e.g., BAMS, SINS, etc.
2. Names of microprocessor data units shall be written with all capital letters, and numbers if any, e.g., XTRAP, WSFX2, NSLR3, FXWS.
3. All of the words in the titles of program subdivisions, except articles, conjunctions, and prepositions, shall be spelled with capital first letters, e.g., Racetrack and Cloverleaf Plot, Beacon Data Dump, Write Program on Magnetic Tape for Recovery.

3.2.2 SECTIONS

Sections are used primarily to subdivide the text of complex or lengthy documents into logical categories both to aid the preparer in organizing the

3.2.2 Continued

material and to aid the user in locating material. Documents should not be over-sectionalized; the exact number and content of each section shall be determined by the nature and extent of the information presented.

Descriptive section headings shall be used, and the sections shall be arranged in an orderly and logical manner.

The section number shall precede all page numbers, paragraph numbers, and figure and table numbers.

3.2.3 FIGURES AND TABLES

As far as possible, figures and tables should be limited to single sheets.

3.2.3.1 FOLDOUTS

Foldouts shall be avoided except where required for legibility.

3.2.3.2 TITLES

If the figure or table occupies more than one page, each page shall contain the same figure or table number and title, and the title shall be followed by the page number and the total number of pages of the figure or table in parentheses, e.g., (page 1 of 3).

3.2.3.3 PLACEMENT

Figures and tables may be placed on or immediately following the page of text on which the first reference is made to the figure or table. If the first reference is accompanied by an explanation, the figure or table may appear immediately following such an explanation.

If figures and tables are numerous and their locations, as indicated above, would interfere with correct sequencing of paragraphs and cause difficulty in understanding or interpretation, they may be placed in a group following a subsection of text or they may be included in a special section after all text.

4.0 MICROPROCESSOR PROGRAM FUNCTIONAL SPECIFICATION

4.1 GENERAL REQUIREMENTS

The Microprocessor Program Functional Specification (MPFS) shall describe in detail all the operational and functional requirements necessary to design and test the microprocessor program.

4.2 DETAILED REQUIREMENTS

For convenience in describing the minimum essential content, the following paragraphs show a normal format for presentation of the material.

Section 1 - Scope.

This MPFS section shall consist of the following paragraphs:

Paragraph 1.1 - Identification .

This MPFS paragraph shall contain the identification of the microprocessor program.

Paragraph 1.2 - Introduction.

This MPFS paragraph shall contain a general discussion of the RSED system within which the program will operate. It shall show the role assigned to the microprocessor program to delineate the functions it must accomplish.

Section 2 - Applicable Documents.

This MPFS section shall list all applicable documents.

Section 3- Requirements.

This section shall define and specify all functional requirements.

Paragraph 3.1 - Functional Description.

This MPFS paragraph

shall provide a detailed description of the major functions of the microprocessor program and shall describe the functional relationships of the microprocessor program with interfacing equipments. This MPFS paragraph shall include the following:

Paragraph 3.1.1 - Microprocessor Interface Block Diagram.

This MPFS paragraph shall contain a block diagram of the equipment/microprocessor relationships to facilitate presentation of material. The diagram shall show the data flow between the microprocessor and the interfacing RSED hybrid equipment.

Paragraph 3.1.2 - Equipment Descriptions. This paragraph shall contain a description of the requirements imposed on the microprocessor program by each interfacing equipment, the purpose of the equipment, and how it is used with the microprocessor.

Paragraph 3.1.3 - Microprocessor Input/Output. This MPFS paragraph shall provide a description of input data derived from sources external to the microprocessor. It will also describe output data given to interfacing equipment by the microprocessor.

Paragraph 3.1.4 - Function Description. This MPFS paragraph shall contain a subparagraph for each function to be supported by the microprocessor program. The descriptions shall provide a brief statement of purpose for each function, as well as text and mathematical descriptions for each of the functions performed by the microprocessor program.

Appendix A - Mathematical Analysis. This MPFS section may be included as an appendix to the Microprocessor Program Functional Specification. It shall include additional mathematical analysis as required to provide a complete comprehension of the RSED system.

5.0 MICROPROCESSOR PROGRAM DESIGN SPECIFICATION

5.1 GENERAL REQUIREMENTS

The Microprocessor Program Design Specification (MPDS) shall specify the design description of the microprocessor program based upon the functional requirements defined in the Microprocessor Program Functional Specification (Section 4). This MPDS shall specify the programming approach for implementing the microprocessor program and shall define how the functions are to be performed.

5.2 DETAILED REQUIREMENTS

For convenience in describing the minimum essential content, the following MPDS paragraphs show a normal format for presentation of the material.

Section 1 - Scope

This MPDS section shall contain the microprocessor program title and provide a brief summary of the purpose and scope of the specification. It shall also contain a description of the major functions of the computer program.

Section 2 - Applicable Documents

This MPDS section shall list the Microprocessor Program Functional Specification, standards, and other documents which apply to the preparation of this specification.

Section 3 - Requirements

This MPDS section shall contain a comprehensive description of the Microprocessor program design structure and processing. The description shall reflect the translation of the microprocessor system functions defined in the Microprocessor Program Functional Specification to the design of the microprocessor program.

Paragraph 3.1 - Function Allocation/Description

This MPDS paragraph shall identify and describe the allocation of functions and tasks to be performed by the individual microprocessor subprograms.

The identification of tasks shall be derived from the requirements in the Microprocessor Program Functional Specification. A description of the design structure (e.g., modular, through-put, segmented) to be implemented for translating the MPFS functions into subprograms shall be defined. This paragraph shall include a general summary of inputs, outputs, and functions to be performed for each subprogram and common subroutine.

Paragraph 3.2 - Microprocessor Program Functional Flow Diagram

This MPDS paragraph shall show the general system flow of both data and control.

Paragraph 3.3 - Storage and Processing Allocation

This MPDS paragraph shall describe the allocation of memory storage and processing time to subprograms, and the data base. The total memory allocation and processing time for each subprogram and common data base shall be summarized.

Paragraph 3.4 - Programming Guidelines

This MPDS paragraph shall specify the programming guidelines to be observed by the system programmer when producing the microprocessor program. This MPDS paragraph shall name the programming language and its supporting system, i.e., monitor, loader, librarian, debug and utilities, that will be used to produce the microprocessor program. The appropriate users manuals and specifications for the language and system shall be referenced. This MPDS paragraph shall state in concise terms the mnemonic

Paragraph 3.4 (Continued)

labeling conventions to be observed.

Section 4 - Detailed Requirements.

This section shall contain for each subprogram and system subroutine, a paragraph 4.N, which develops and completely defines the subprogram/system subroutine. Each 4.N paragraph will contain subparagraphs as follows:

Paragraph 4.N.1 - Subprogram Detailed Description

This MPDS paragraph shall specify the design of the subprogram in detail.

It shall describe completely the processing requirements of the subprogram.

This paragraph shall contain a textual development of the operations performed by the subprogram and shall describe each section of code as it appears (or will eventually appear) in the subprogram listing. This, in essence, will describe the operations performed at each branch of the subprogram, and the results obtained by following each branch.

During the discussion of subprogram segments, if common system subroutines are used, they shall be identified by their function and mnemonic label with a reference to the paragraph where they are described in detail.

The level of detail for this portion of the MPDS amplifies the information provided in the subprogram flow diagrams described in the following MPDS paragraph 4.N.2. The same subprogram tags specified in the text description shall be shown in the appropriate blocks of the related flow diagrams.

Paragraph 4.N.2 - Subprogram Flow Diagrams

A flowchart shall be included which depicts detailed operations performed by the microprocessor subprogram.

Paragraph 4.N.3 - Microprocessor Subprogram Environment

This MPDS paragraph shall contain a general description of the subprogram environment.

Paragraph 4.N.3.1 - Tables

This MPDS paragraph shall contain the detailed description of each table used only in the subprogram/system subroutine data base. Each table shall be described individually, where the descriptions are presented according to the alphabetically ordered mnemonic table names. The minimum content of the subprogram table descriptions shall be:

- a. Table Name
- b. Purpose and Type
- c. Size and Indexing Procedure
- d. Structure and Bit Layout

Paragraph 4.N.3.2. - Variables

This MPDS paragraph shall contain the detailed description of each variable included in the subprogram/system subroutine data base. Each variable shall be described individually where the descriptions are presented according to the alphabetical ordering of the mnemonic names of the variables. The minimum content of this MPDS paragraph shall be:

- a. Variable Name
- b. Purpose
- c. Structure and Bit Layout

Paragraph 4.N.3.3 - Constants

This MPDS paragraph shall contain the detailed description of each constant included in the subprogram/system subroutine data base. Each constant shall be described individually, where the descriptions are presented according to the alphabetical ordering of the mnemonic names of the flags. The minimum

Paragraph 4.N.3.3 (Continued)

content of this MPDS paragraph shall be the following information:

- a. Constant Name
- b. Purpose and Status
- c. Structure and Bit Layout

Paragraph 4.N.3.4 - Flags

This MPDS paragraph shall contain the detailed description of each flag included only in the subprogram/system subroutine data base. Each flag shall be described individually, where the descriptions are presented according to the alphabetical ordering of the mnemonic names of the flags. The minimum content of the MPDS paragraph shall be the following information

- a. Flag Name
- b. Purpose and Status
- c. Structure and Bit Layout

Paragraph 4.N.3.5 - Indexes

This MPDS paragraph shall contain the technical description of each index included in the subprogram/system subroutine data base. Each index shall be described individually where the descriptions are presented according to the alphabetical ordering of the mnemonic names of the indexes. The minimum content for this MPDS paragraph shall be:

- a. Index Name
- b. Purpose

Paragraph 4.N.3.6 - Common Data Base Reference

This MPDS paragraph shall provide a complete list of all common data base items referenced by each subprogram/system subroutine. This list provides a cross reference to the Common Data Base section which provides the technical description of the common data base items.

Paragraph 4.N.4 - Input/Output Formats

This MPDS paragraph shall contain a description of each input and output processed by the subprogram/system subroutine.

Paragraph 4.N.5 - Conditions for Initiation

This MPDS paragraph shall identify system conditions that must be met for this subprogram/system subroutine to be initiated for processing. For those subprograms/system subroutines that are always initiated for processing regardless of system conditions, the word "UNCONDITIONAL" shall be shown. For those subprograms that are initiated due to one or more unique conditions, each possible condition or set of conditions shall be described. If the conditions are based on the settings of certain items of information, each item, its required value, and a definition (or reference) of that value shall be shown.

Paragraph 4.N.6 - Subprogram / System Subroutine Limitations

This MPDS paragraph shall summarize any known or anticipated limitations of the subprogram/system subroutine. A list of all restrictions and constraints that apply to the subprogram/system subroutine shall be provided, including timing requirements, limitations of algorithms and formulas used, and design limits of input and output data.

Paragraph 4.N.7 - Interface Description

This MPDS paragraph and an associated block diagram shall show the sequential and functional relationship of the subprogram with the other subprograms and system subroutines with which it interfaces.

Section 5 - Common Data Base.

This section shall provide a complete detailed description of all data items necessary to carry out the functions of the microprocessor program. Common data is that data required by two or more subprograms or system subroutines. Examples of common data include constants, indexes, flags, variables and tables.

Paragraph 5.1 - Tables

This MPDS paragraph shall contain the detailed description of each table used in the common data base. Each table shall be described individually where the descriptions are presented according to the alphabetical ordering of the mnemonic name of the table. The minimum content of this paragraph shall be the following information:

a. Table Name

The title of the table with the assigned mnemonic label in parenthesis, e.g., Common Track Table (CDTRK).

b. Purpose and Type

The table type (e.g., fixed or variable length, table structure) and the explicit use of the table.

c. Size and Indexing Procedure

The number of items in the table and the number of microprocessor words required by each item. It shall also define, in precise terms, the method used to index through the various items of the table and any special conditions pertaining to the referencing of an included item.

d. Field Name

The title of the field with the assigned mnemonic in parenthesis.

e. Purpose and Type

An explicit description of the use of the field, and indication of its type (e.g., alphanumeric integer, fixed point or floating point).

f. Size

The size of the field in words or bits.

g. Binary Point

This information shall be included for all numeric type fields except floating point, and shall indicate the bit position of the binary

Paragraph 5.1 (Continued)

point (scaling) of the variable.

h. Range of Values and Initial Condition

The minimum and maximum values that are valid for the field, and the initial condition of the field if it is preset. For alphanumeric types the data code (e.g., ASCII, BCD) shall also be given.

i. Static/Dynamic

The changeability nature of the field (e. g., unchanging value is static, changing field values are dynamic).

j. Structure and Bit Layout

A diagram for each microprocessor word required by the field.

Paragraph 5.2 - Variables

This MPDS paragraph shall contain the detailed description of each variable included in the common data base. Each variable shall be described individually, where the descriptions are presented according to the alphabetical ordering of the mnemonic names of the variables.

The minimum content of this paragraph shall be the following information:

- a. Variable Name
- b. Purpose and Type
- c. Size - number of bits and sign
- d. Binary Point (not applicable to floating point numeric or alphanumeric types)
- e. Range of Values and Initial Condition
- f. Static/Dynamic
- g. Structure and Bit Layout

Paragraph 5.3 - Constants

This MPDS paragraph shall contain the detailed description of each constant included in the common data base. Each constant shall be described individually, where the descriptions are presented according to the alphabetical ordering of the mnemonic names of the constants. The minimum content of this paragraph shall be the following information:

- a. Constant Name
- b. Purpose
- c. Initial Condition
- d. Structure and Bit Layout

Paragraph 5.4 - Flags

This paragraph shall contain the detailed description of each flag included in the common data base. Each flag shall be described individually, where the descriptions are presented according to the alphabetical ordering of the mnemonic names of the flags. The minimum content of this paragraph shall be the following information:

- a. Flag Name
- b. Purpose
- c. Initial Condition
- d. Structure and Bit Layout

Paragraph 5.5 - Indexes

This paragraph shall contain the detailed description of each index included in the common data base. Each index shall be described individually, where the descriptions are presented according to the alphabetical ordering of the mnemonic name of the index. The minimum content of this paragraph shall include the following information:

- a. Index Name
- b. Purpose

Paragraph 5.6 - Subprogram Reference (Set/Used)

This MPDS paragraph shall include a complete list of all common data base items with a cross reference which includes all referencing subprograms/system subroutines.

Paragraph 5.7 - Notes

This MPDS section shall include a list of all subprograms/system subroutines by text name and mnemonic. The order of the list shall be in an alphabetical arrangement based upon the identifying mnemonic labels.

Appendix B

This MPDS paragraph shall include any information which is too bulky to be placed in the body of the document.

SPECIFICATION FOR RSED MICROPROCESSOR

(BREADBOARD VERSION)

SPECIFICATION NO. RS - 16

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1.0 Introduction

This specification describes the requirements for the Microprocessor that is part of the Reed-Solomon Encoder/Decoder.

1.1 Function

The Microprocessor shall accept a data block representing header information, data characters, parity characters, S_K syndromes, number of erasures, erasure locations (compact) and shall compute the erasure location polynomial, modified syndromes, error location polynomial, error location calculator, errata value calculator and shall output a data block representing header (with errata number) and corrected data and parity characters. The Microprocessor shall also provide two words within the DATA RAM used per data block (A & B) for data steering and completion of the decoding process.

2.0 Applicable Documents

<u>Document Name</u>	<u>Number</u>
RS Glossary	RS-3
*RS Output/Input Blocks	RS-4
RS α (Alpha) Definition	RS-8
*RS Hardware Functional Spec	RS-9
*RS Software Functional Spec	RS-10

Data Sheets for Intel 3001, 3002, 3003

*Updated by this document.

3.0 Definitions

RSED Reed Solomon Encoder/Decoder

SLL Standard Logic Level

4.0 Performance Requirements

The electrical performance shall be met over the environmental conditions specified below.

Temperature-Operating

Commercial Parts 0°C to +70°C

Military Parts -55°C to +125°C

4.1 Inputs

4.1.1 Power Supplies

To be determined.

4.1.2 RAM Data Blocks

4.1.3 ROM Inputs from ROM Simulator

4.1.4 Interface from Test Panel

4.1.6 Software

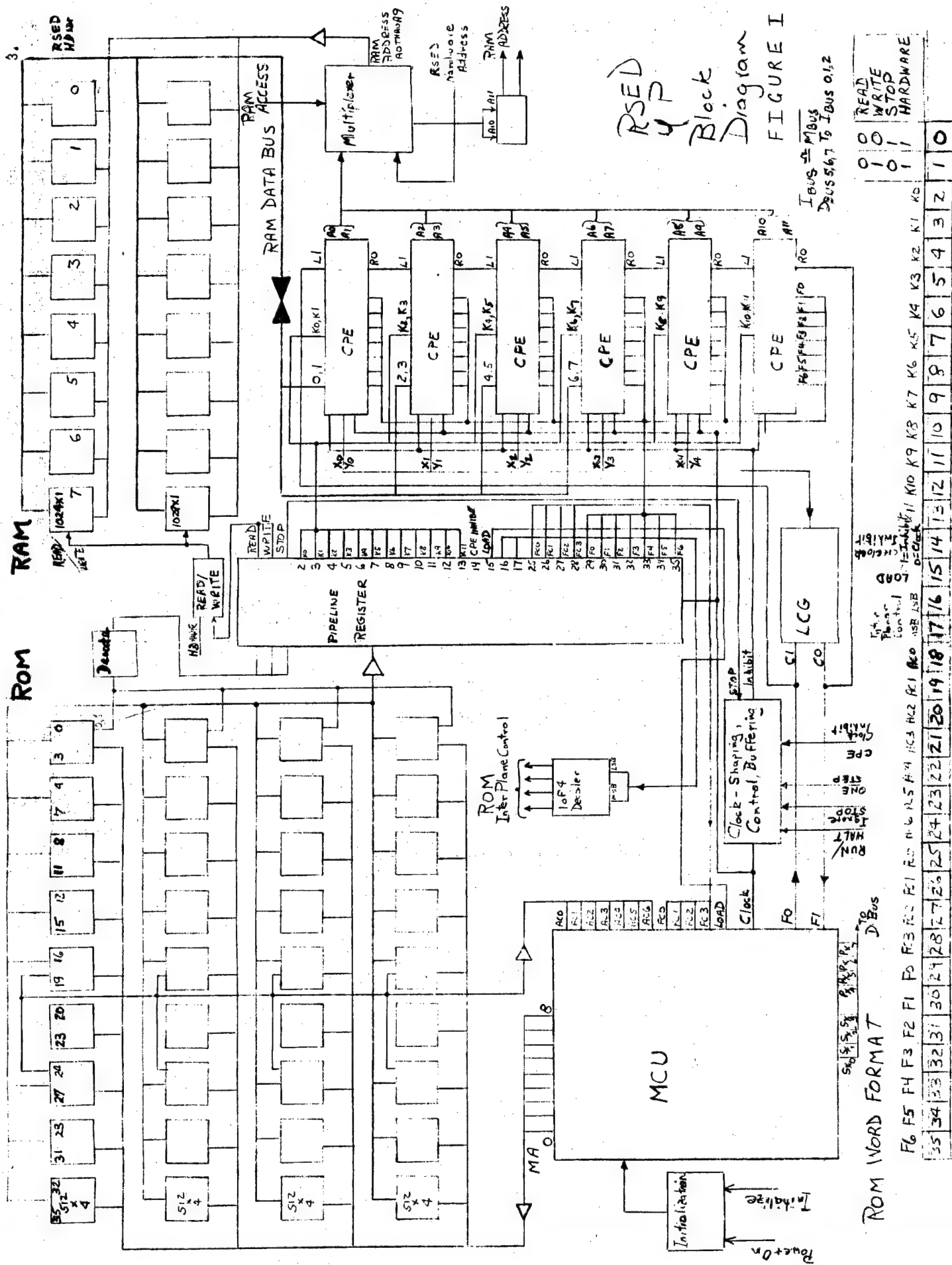
4.2 Outputs

4.2.1 RAM Data Blocks

4.2.2 Interface from Test Panel

4.3 Internal Characteristics (Hardware)

The RSED Microprocessor section of the RSED hardware shall consist of the following elements (see Figure 1) per Microprocessor.



4.3 Internal Characteristics (Hardware) (continued)

- a. Microprogram Control Unit (MCU)
- b. Central Processing Element (CPE). Six required.
- c. Look-Ahead Carry Generator (LCG)
- d. PROM Memory 2048 x 36 using 512 x 4 building blocks.
- e. RAM Memory 2048 x 8 using 1024 x 1 building blocks.
- f. Pipe Line Register
- g. 25 MHz Oscillator
- h. Clock Shaping, Control and Buffering
- i. RAM Address Multiplexer and Buffering
- j. RAM Data Multiplexer and Buffering

The microcomputer devices shall be selected from a family of Schottky bipolar LSI circuits (3000 series). Interface devices shall be compatible with the 3000 series (speed and loading). Initially, limited temperature range (0°C to 70°C) INTEL devices may be utilized for breadboard check-out. Eventually the limited temperature range devices shall be replaced with military temperature range (-55°C to +125°C) devices. Limited and full temperature range devices must be pin for pin compatible.

4.3.1 Microprogram Control Unit (3001)

The 3001 Microprogram Control Unit (MCU) controls the sequence in which microinstructions are fetched from the microprogram memory. Its functions include the following (Reference Figure 2):

- Maintenance of the microprogram address register.

- Selection of the next microinstruction based on the contents of the microprogram address register. (Refer to Pipe Line Register for plan or addressing).

3001 Block Diagram

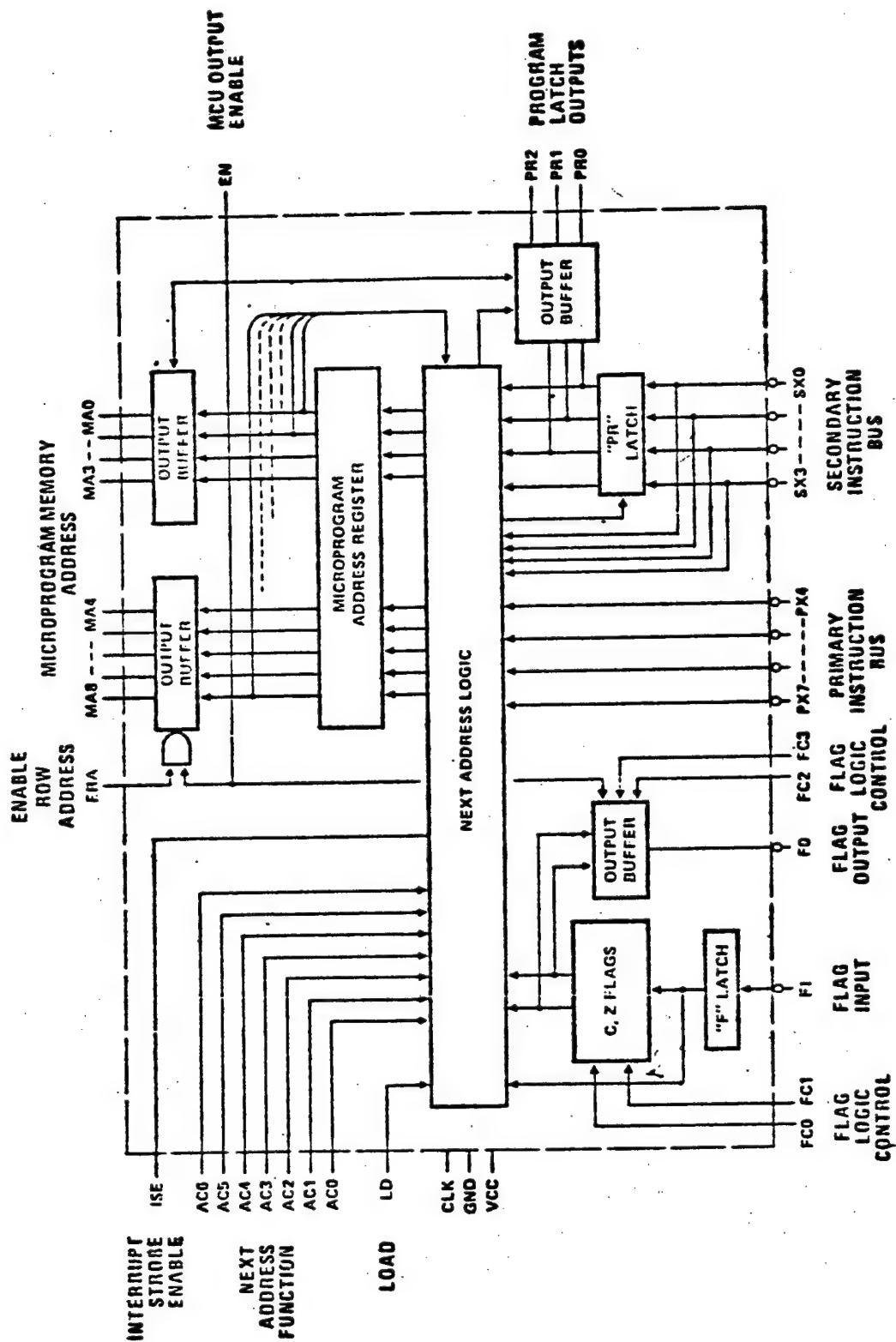


FIGURE 2 MCU

4.3.1 Microprogram Control Unit (3001) (continued)

Decoding and testing of data supplied via several input busses to determine the microinstruction execution sequence. Saving and testing of carry output data from the central processor (CP) array.

Control of carry/shift input data to the CP array.

Control of microprogram interrupts.

4.3.2 Central Processing Elements (3002)

The 3002 Central Processing Element contains all of the circuits that represent a 2 bit wide slice through the data processing section of a digital computer. To construct a complete central processor for a given word width N , it is simply necessary to connect an array of $N/2$ CPE's together. When wired together in such an array, a set of CPE's provide the following capabilities. (Reference Figure 3).

2's complement arithmetic

Logical AND, OR, NOT and exclusive - OR

Incrementing and Decrementing

Shifting left or right

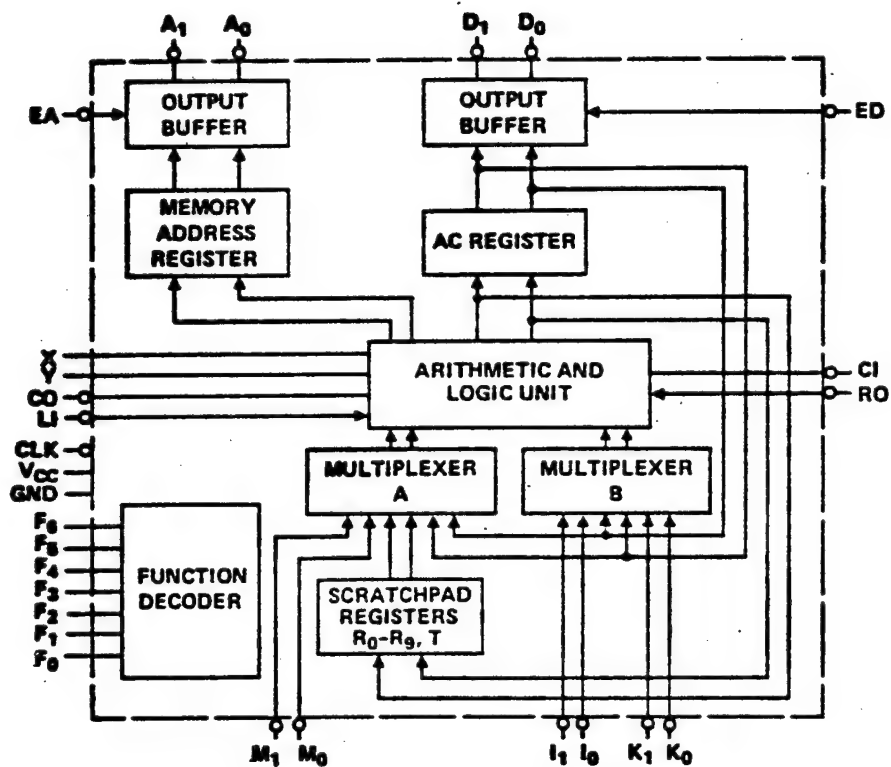
Bit testing and zero detection

Carry look-ahead generation

Multiple data and address busses

4.3.3 Look-Ahead Carry Generator (3003)

The 3003 Look-Ahead Carry Generator (LCG) is a high speed circuit capable of anticipating a carry across a full 16 bit 3002 Central Processing Array. The LCG accepts light pairs of active high cascade inputs (X, Y) and an active low carry input and generates active low



3002 BLOCK DIAGRAM

FIGURE 3 CPE

4.3.3 Look-Ahead Carry Generator (3003)

carries for up to eight groups of binary adders. The Look-Ahead Carry Generator shall be connected to the CPEs to provide a normal arithmetic carry.

4.3.4 ROM Memory 2048 x 36^{*}

Initial μ P checkout (software) shall be accomplished with the aid of a ROM simulator. The ROM simulator shall be organized in blocks of 512 x 4 memory sections. A total memory capacity of 2048 x 36 is required (36-512x4). The ROM simulator shall have an access time of 100 nanoseconds. The final PROM's used with the μ P shall have a maximum access time of 60 com/80 mil nanoseconds under worst conditions.

4.3.5 RAM Memory 2048 x 8^{*}

A RAM Memory (2048 x 8) shall be incorporated into the μ P design. The memory shall be made up of 1024 x 1 circuits. Maximum RAM access time shall be 45 com/70 mil. nanoseconds under worst case conditions.

4.3.6 Pipe Line Register

A pipe line register (see Figure 1) shall be provided. The output of the register contains the bit pattern of the current instruction being executed.

The following bits shall be wired into the pipe line register:

READ

WRITE

STOP

Ko thru K11

CPE Inhibit

*Complete checkout requires testing using military devices at room temperature.

4.3.6 Pipe Line Register (continued)

Load

Inter Planar Control MSB and LSB

FO through F6

FCO through FC3

4.3.7 Decode

Bits 0 and 1 of the microinstruction shall be decoded as per Figure 1 description.

4.3.8 Clock Shaping, Control and Buffering

A section of the microprocessor hardware shall provide the basic micro-computer clock and clock control circuits as well as required buffering.

A 25 MHz crystal controlled oscillator shall be utilized to obtain the various clocks required. The microcomputer clock shall be 200 nanosec. with a duty cycle as specified in Intel data sheets.

The following controls shall be incorporated into the microprocessor control section.

Run/Halt - Enables/Disables the microprocessor clock.

One Step - Every time this control is activated the program advances one step (one micro instruction).

Ignore Stop - This control overrides programmed stops.

4.3.9 Initialization

With power turn on or when an initialization control is activated, the following initialization steps take place in each microprocessor simultaneously:

- a. The ROM memory address is set to plane 0, ROW 0, Column 15.

4.3.10 Sx and Px Bus Inputs

The primary and secondary bus inputs of the MCU shall be wired as follows:

Sx_0	to	D0
Sx_1	to	D1
Sx_2	to	D2
Sx_3	to	D3
Px_4	to	D4
Px_5	to	D5
Px_6	to	D6
Px_7	to	D7

4.3.11 External Bus Inputs (I Bins)

The external bus (I) inputs shall be wired as follows in Figure 4.

The following connections shall be made to the I bus as listed below:

Microinstruction

Bits	
<u>1</u>	<u>0</u>
1	1
0	1

M bus is set to logic level "0"

I Bus bits 3, 4, 5, 6 and 7 are set logic level "0"

I Bus bits 0, 1, 2 are set to the states of the D Bus

5, 6, 7 that is

$$I_0 = D5$$

$$I_1 = D6$$

$$I_2 = D7$$

0 0
or

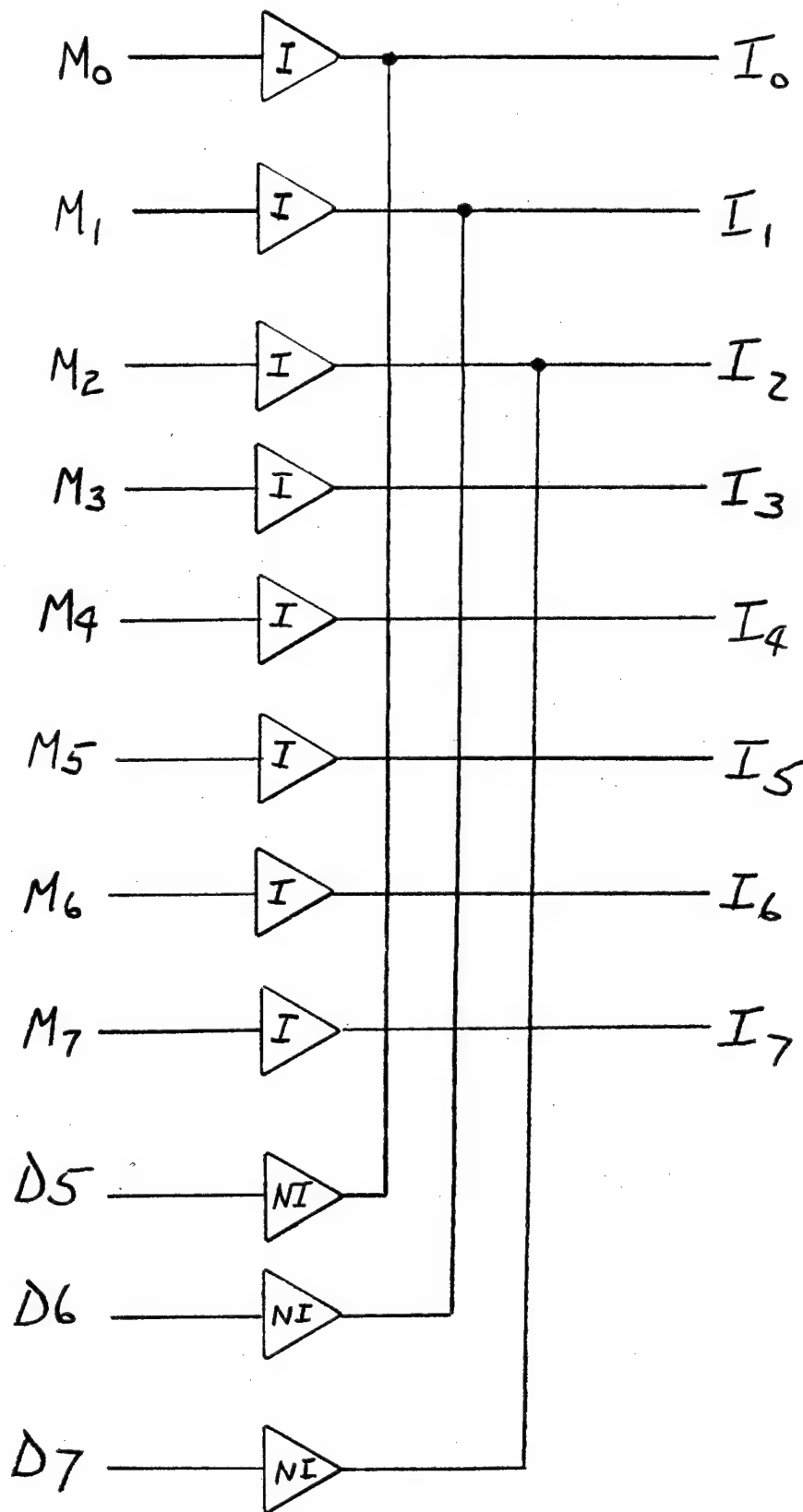
1 0

M Bus is enabled, the I Bus is set to logic inversion of

the M Bus and the D Bus is turned off (that part that connects

to the I Bus).

A76



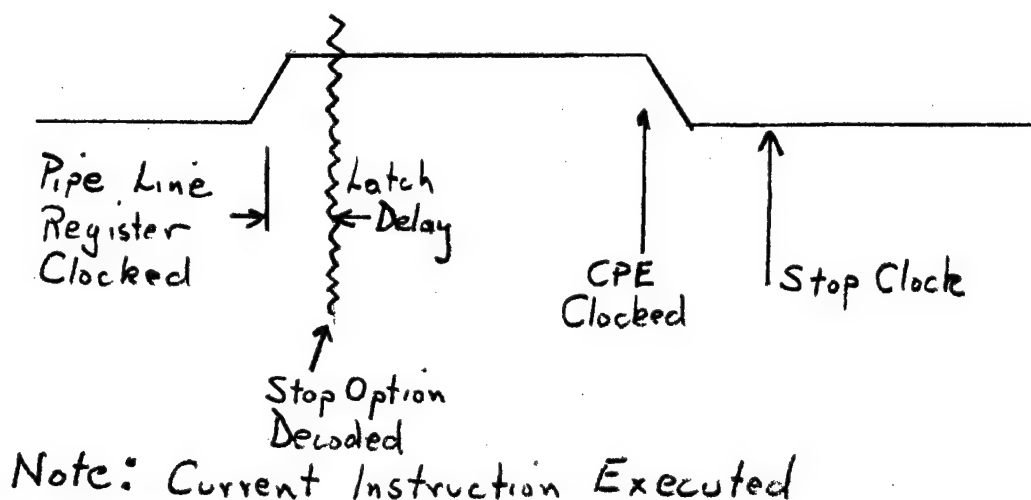
External Bus Inputs
(I Bus)

Figure 4

I Inverting
 NI Non Inverting

4.3.12 Programmed Stop

When an instruction is clocked into the pipeline register with bits 0, 1 set to logic level "1" and "0" respectively (see Figure 1) the stop function is enabled, the CPE is clocked and the clock is disabled after the positive to negative transition of the clock (clock will remain at logic level "0").

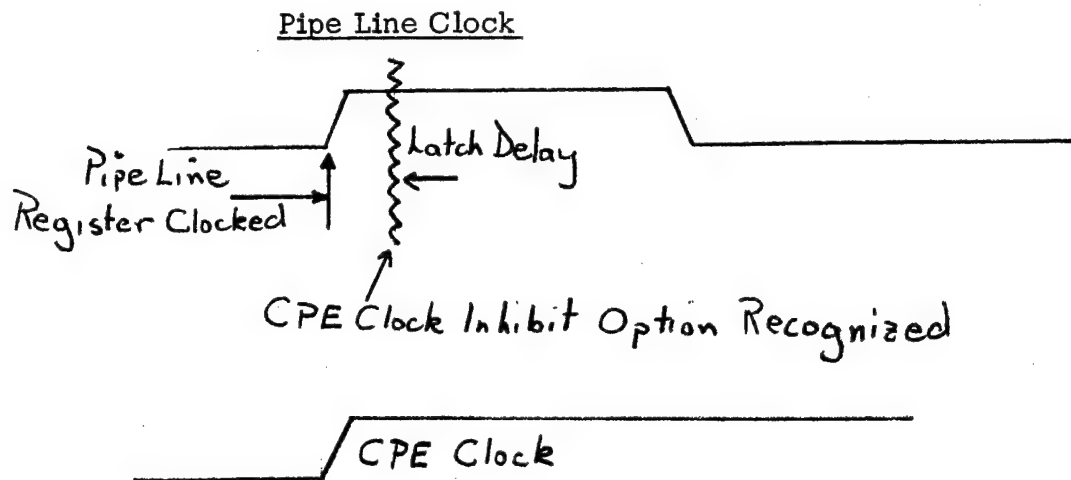


4.3.13 CPE Clock Inhibit

When an instruction is clocked into the pipeline register with bit 14 set to logic level "1" (see Figure 1) the clock to the CPEs shall not be allowed to transition from logic level "1" to logic level "0" for the instructions that have bit 14 (micro instruction) set to logic level 1.

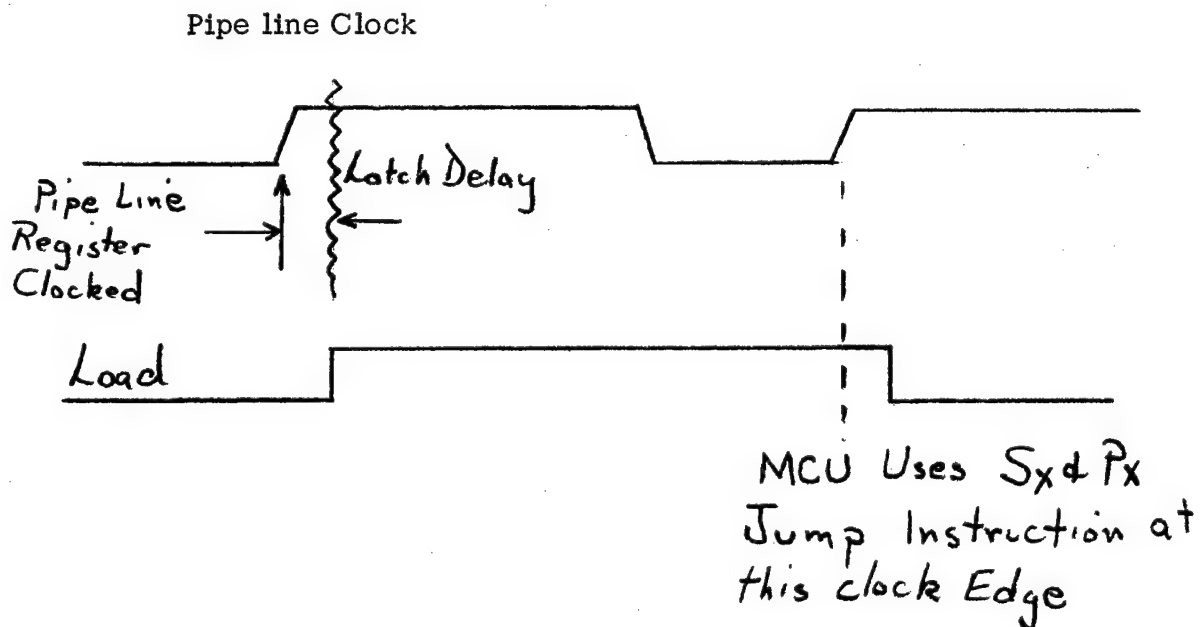
The instructions not requiring the CPE clock will be executed and the registers will be left unchanged.

4.3.13 CPE Clock Inhibit (continued)



4.3.14 Load

When an instruction is clocked into the pipe line register with bit 15 set to logic level "0" a load pulse shall be generated that enables the data on the D Bus to be entered into the MCU via the S_x and P_x Bus.



4.3.15 Logic Level Definitions

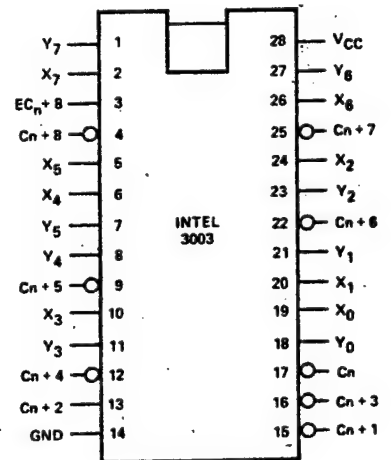
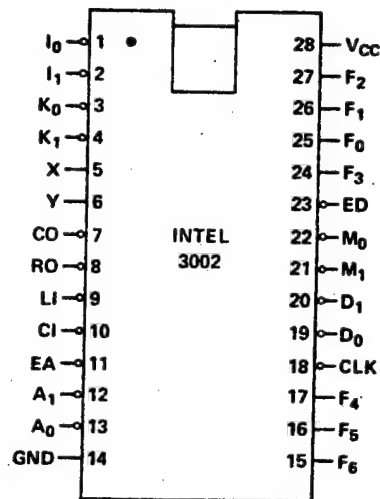
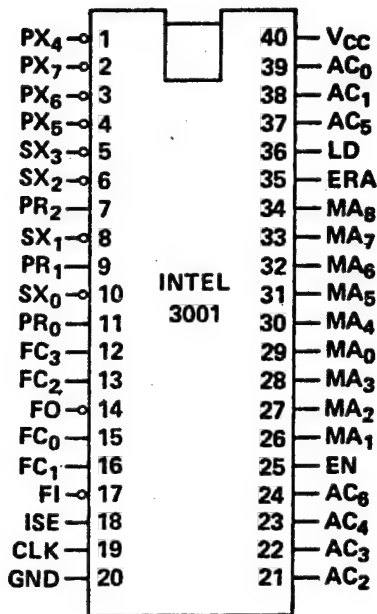
Intel data sheets for 3001, 3002 and 3003 circuits have an active high and active low states for the various input and output signals.

Active Low

Refer to layouts below. An active low signal represented by $\text{---}0$

is defined as follows: Logic Level "0" is equivalent to +3V.

Logic Level "1" is equivalent to 0V.



Active High

An active high signal is defined as follows:

Logic Level "0" is equivalent to 0V.

Logic Level "1" is equivalent to +3V.

DATA RAM INPUT/OUTPUT WORD FORMAT

Table 1

RAM ADDRESS	BIT POSITION						DESCRIPTION	
	* 5	4	3	2	1	0		
0 1 2 3							UNALLOCATED	
4		Word # Bit 0	Block # MSB	Block # LSB	0-Valid 1-Invalid	Code Select	Header	
5		Word # Bit 5	Word # Bit 4	Word # Bit 3	Word # Bit 2	Word # Bit 1	Header	
6		Debug Flag	Debug Flag	Word # Bit 8	Word # Bit 7	Word # Bit 6	Header	
7		Errata MSB	Errata	Errata	Errata	Errata LSB	Header	
8		MSB				LSB	31/15 C30	16/4 "0"s
9		MSB				LSB	C29	"0"s
10		MSB				LSB	C28	"0"s
11		MSB				LSB	C27	"0"s
12		MSB				LSB	C26	"0"s
13		MSB				LSB	C25	"0"s
14		MSB				LSB	C24	"0"s
15		MSB				LSB	C23	"0"s
16		MSB				LSB	C22	"0"s
17		MSB				LSB	C21	"0"s
18		MSB				LSB	C20	"0"s
19		MSB				LSB	C19	} DATA
20		MSB				LSB	C18	
21		MSB				LSB	C17	
22		MSB				LSB	C16	
23		MSB				LSB	C15	Parity A81

* See last chart page.

DATA RAM INPUT/OUTPUT WORD FORMAT

Table 1 (contd.)

RAM ADDRESS	BIT POSITION						DESCRIPTION	
	*5	4	3	2	1	0		
24		MSB				LSB	31/15 C14	16/4
25		MSB				LSB	C13	
26		MSB				LSB	C12	
27		MSB				LSB	C11	
28		MSB				LSB	C10	
29		MSB				LSB	C09	PARITY
30		MSB				LSB	C08	
31		MSB				LSB	C07	
32		MSB				LSB	C06	
33		MSB				LSB	C05	
34		MSB				LSB	C04	
35		MSB				LSB	C03	
36		MSB				LSB	C02	4 Erasures
37		MSB				LSB	C01	
38		MSB				LSB	C00	
39		MSB				LSB	SPARE	
40		MSB				LSB	S1	
41		MSB				LSB	S2	Syndromes
42		MSB				LSB	S3	
43		MSB				LSB	S4	
44		MSB				LSB	S5	
45		MSB				LSB	S6	A82

*See last chart page.

DATA RAM INPUT/OUTPUT WORD FORMAT

Table 1 (contd.)

RAM ADDRESS	BIT POSITION						DESCRIPTION
	*5	4	3	2	1	0	
46							
		MSB				LSB	S7
47							
		MSB				LSB	S8
48							S9
49							S10 Syndromes
50							S11
51							S12
52							S13
53							S14
54							S15
55							S16
56							
		MSB				LSB	Number of Erasures
57							31/15 16/4
58							E_L
59							1. There are as many E_L 's as there are erasures.
60							2. The E_L 's are packed
61							
62							3. The E_L 's are in descending order
63							
64							4. The maximum number of E_L 's is 31.
65							
66							
67							
68							A83

*See last chart page.

DATA RAM INPUT/OUTPUT WORD FORMAT

Table 1 (contd.)

RAM ADDRESS	BIT POSITION						DESCRIPTION
	* 5	4	3	2	1	0	
69							
70							
71							
72							
73							
74							
75							
76							
77							
78							
79							
80							
81							
82							
83							
84							
85							
86							
87							
88							Unallocated
89							
90							
	*See last chart page.						

DATA RAM INPUT/OUTPUT WORD FORMAT

Table 1 (cont'd.)

RAM ADDRESS	BIT POSITION						DESCRIPTION
	* 5	4	3	2	1	0	
91							Unallocated
92							
93							
94							
95							
96							
97							
98							
99							
100							
101							
102							
103							
104							
105							
106							
107							
108							
109							
110							
111							
112							
113	*See last chart page.						A85

DATA RAM INPUT/OUTPUT WORD FORMAT

Table 1 (contd.)

RAM ADDRESS	BIT POSITION						DESCRIPTION
	* 5	4	3	2	1	0	
114							Unallocated
115							
116							
117							
118							
119							
120							
121							
122							
123							
124							
125							
126						X	A Read
127					Z	Y	A Write
	<p>* Words at RAM address 8 through 38 bit position.</p> <p>5 is used for erasure determination.</p> <p>"1" = erasure</p> <p>0 = valid character</p> <p>Address 0 through 127 - Input/Output Area A</p> <p>128 through 255 - Input/Output Area B (Same format as A)</p>						

READ/WRITE CONTROL

	<u>FLAG</u>	<u>MEANING</u>	<u>SET</u>
126	$\begin{cases} X = 0 \\ X = 1 \end{cases}$	Data not ready Data ready	DSCU (on read completion) Microprocessor (on decode completion)
127	$\begin{cases} ZY = 00 \\ ZY = 01 \\ ZY = 11 \\ ZY = 10 \end{cases}$	No write request made	Microprocessor (when processing begins)
		Write request made (DSCU may write)	Microprocessor (write early)
		DSCU has filled input buffer	DSCU (on write completion)
		Not used	

APPENDIX B

STATISTICAL DISTRIBUTION OF CORRECTABLE ERROR/ERASURE
PATTERNS FOR A (31, 15) REED-SOLOMON CODEWORD

STATISTICAL DISTRIBUTION OF CORRECTABLE ERROR/ERASURE PATTERNS FOR A

(31, 15) REED-SOLOMON CODEWORD

I. INTRODUCTION

The JTIDS II concatenated coded data link is comprised of an M'ary error/erasure inner code channel and a (31, 15) Reed Solomon (RS) outer code channel. The utility of this scheme depends not only on its high performance capability, but also on the required decoding time for received message codewords. While a worst case decoding time can be estimated from the maximum number of correctable errors and erasures, a more realistic value for the average decoding time requires a knowledge of the relative frequency of occurrence of the different errata patterns and the time to decode each pattern. This study addresses the determination of the elemental and cumulative probabilities of various errata patterns, under optimum jamming conditions and for certain specified message reliability levels.

Use or disclosure of this data is subject to the restriction on the Title Page of this Document.

II. ANALYSIS AND RESULTS

An (N, K) RS code can correct up to the number of errata satisfying the relation:

$$2t + s \leq N - K \quad (1)$$

where t and s are the number of character errors and erasures, respectively. Thus, for the (31, 15) code, the probability of correctly decoding a received codeword is given by:

$$Q_w = \sum_{t=0}^8 \sum_{s=0}^{16-2t} \binom{31}{t,s} p_e^t p_E^s (1 - p_e - p_E)^{31-t-s} \quad (2)$$

where p_e and p_E are the inner channel error and erasure transition probabilities, respectively.

From (2), the probability of any specific errata pattern, i.e. $t = t_1$ and $s = s_j$ is:

$$P(t, s) \triangleq P(t = t_1, s = s_j) \quad (3)$$

$$= \binom{31}{t_1, s_j} p_e^{t_1} p_E^{s_j} (1 - p_e - p_E)^{31-t_1-s_j} \quad (4)$$

The normalized value of this errata pattern is defined as

$$P_n(t, s) = \frac{P(t, s)}{Q_w} \quad (5)$$

The normalized probability of receiving a correctable pattern with $t = t_1$ errors is obtained by summing (5) over all values of erasures satisfying (1), or

$$P_{qn}(t) \triangleq P_{qn}(t = t_1) \quad (6)$$

$$= \sum_{s=0}^{16-2t_1} P_n(t, s) \quad (7)$$

The normalized cumulative probability of a correctable errata pattern with $t = t_1$ or less errors is obtained by summing (6) over $t \leq t_1$, or

$$Q_n(t \leq t_1) = \sum_{t=0}^{t_1} P_{qn}(t) \quad (8)$$

In another technical memorandum*, optimum jammer strategies were derived for this data link operating at various codeword reliability levels.

These jammer strategies correspond to specific average values of erasure and error probabilities \bar{p}_E and \bar{p}_e , for the inner channel, which are used in (4) to determine the errata pattern probabilities. Table 1 gives the correspondence between two levels of codeword loss rate, $P_W = 1 - Q_W$, and the transition probabilities.

TABLE I

P_W	\bar{p}_E	\bar{p}_e
5×10^{-4}	0.196	0.0157
10^{-3}	0.214	0.0175

Figures 1, 2, and 3 show plots of equations (5), (7) and (8), respectively, for $P_W = 5 \times 10^{-4}$. Similarly, Figures 4, 5 and 6 show these same plots for $P_W = 10^{-3}$. In addition, Figures 3 and 6 show how the cumulative probability $Q_n(t \leq t_i)$ varies with receiver normalized erasure threshold setting variations due to AGC measurement errors.

* "Optimization of Jammer and Receiver Strategies for a Concatenated Coded Data Link with an Erasure/Error Inner Channel" Advanced CNI Systems Group, CNI Engineering ITT, Avionics Division, Nutley, N.J., August 1975

In Figures 1 or 4, loci for patterns with a constant number of erasures and a variable number of errors are drawn. Only the points on the curves, corresponding to integer values of t_i , are significant. The highest probabilities are obtained for errata patterns with 5 and 6 erasures. For any value of s_j , the probabilities decrease with an increasing number of errors t_i .

Figures 2 and 5 are obtained by adding the probabilities along each vertical line (i.e. for each t_i) in Figure 1 and 4. It gives the total probability of all correctable errata patterns for each value of the number of permissible errors.

In Figures 3 and 6, at the optimum normalized threshold setting of $T_n = 3.5$, the circled points correspond to the partial sums of (8) (or figures 2 and 5) for each $t=t_i$. For example, for $P_W = 5 \times 10^{-4}$, approximately 60 percent of the correctable patterns will have zero errors and 91 percent will have no more than one error. The number of erasures in each case includes all values satisfying (1). The remaining curves in Figure 3 and 6 show how these probabilities vary with T_n .

III. CONCLUSIONS

Probability data has been determined for all correctable RS codeword errata patterns. This data may serve as weighting functions to compute the average decoding time for a received codeword by the RS decoder being built by ITT Avionics, on another contract. If $T(t, s)$ is the time to decode a particular errata pattern of t errors and s erasures, then the average time to decode a word is given by:

$$T_{AVE} = \sum_{t=0}^8 \sum_{s=0}^{16-2t} P_n(t, s) T(t, s) \quad (9)$$

5.

where $P_n(t, s)$ is given in Figure 1 or 4 and $T(t, s)$ may be estimated from the RS decoding algorithm and hardware implementation. A simplified calculation may also be made using the cumulative probabilities in Figures 2 or 5 and the decoding time for the maximum tolerable number of erasures for each t_i , or

$$T_{AVE} < \sum_{t=0}^8 P_{qn}(t) T(t, s=16-2t) \quad (10)$$

gives an upper bound on the average decoding time.

Use or disclosure of this information is subject to the restriction on the Title Page of this Document.

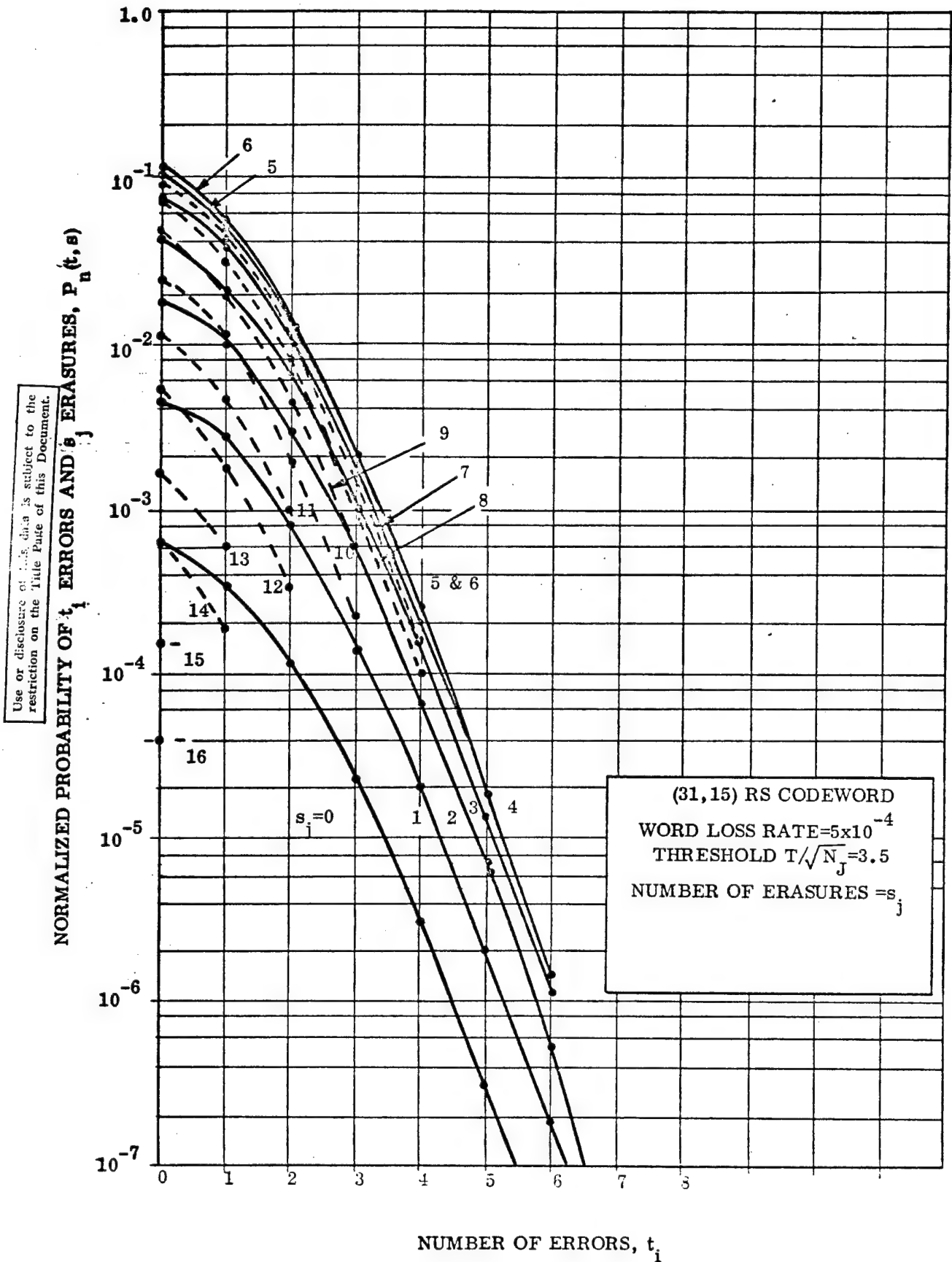


Figure 1. Errata Pattern Probabilities

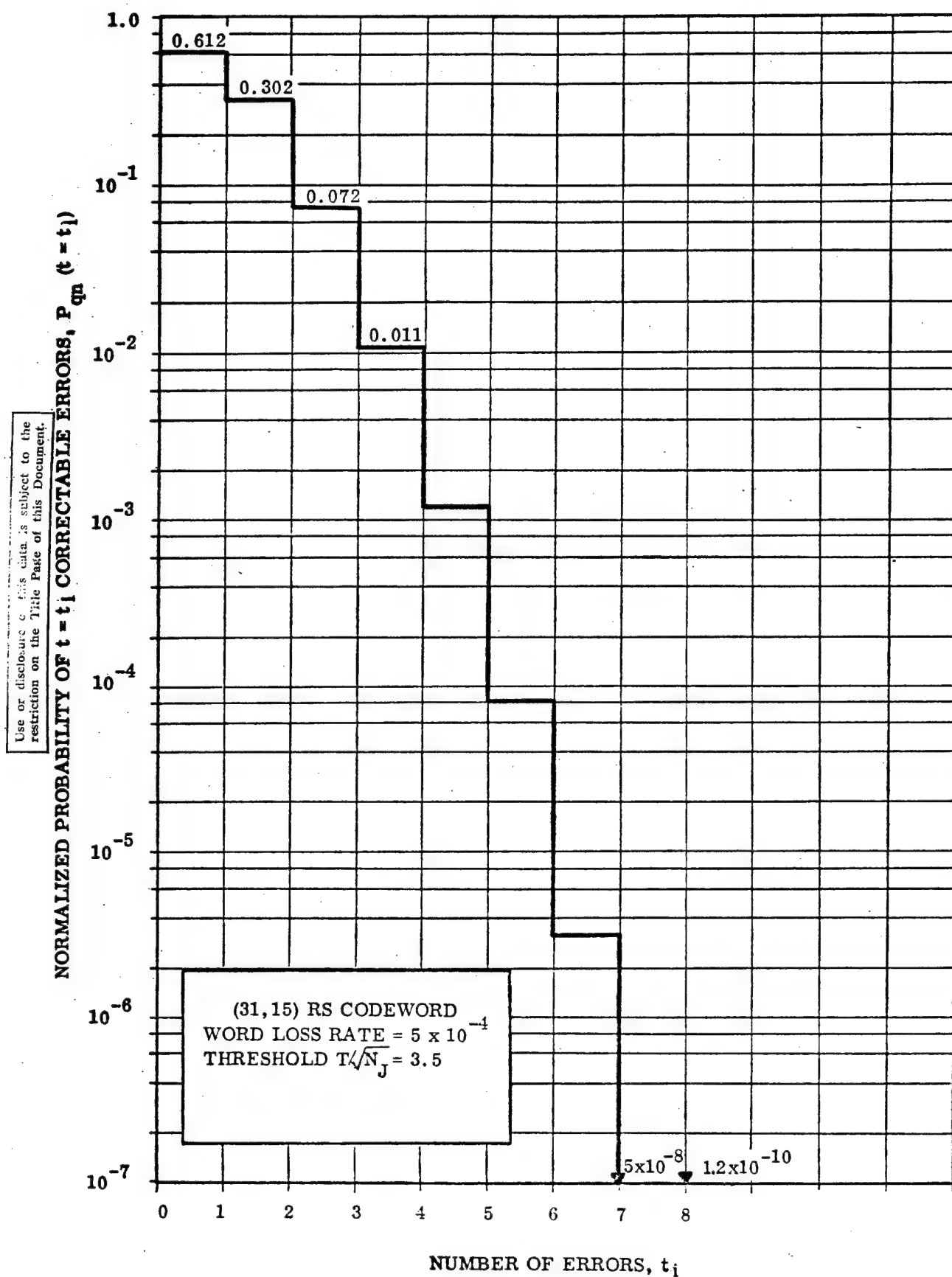


Figure 2. Probability of Correctable Patterns With $t = t_i$ Errors

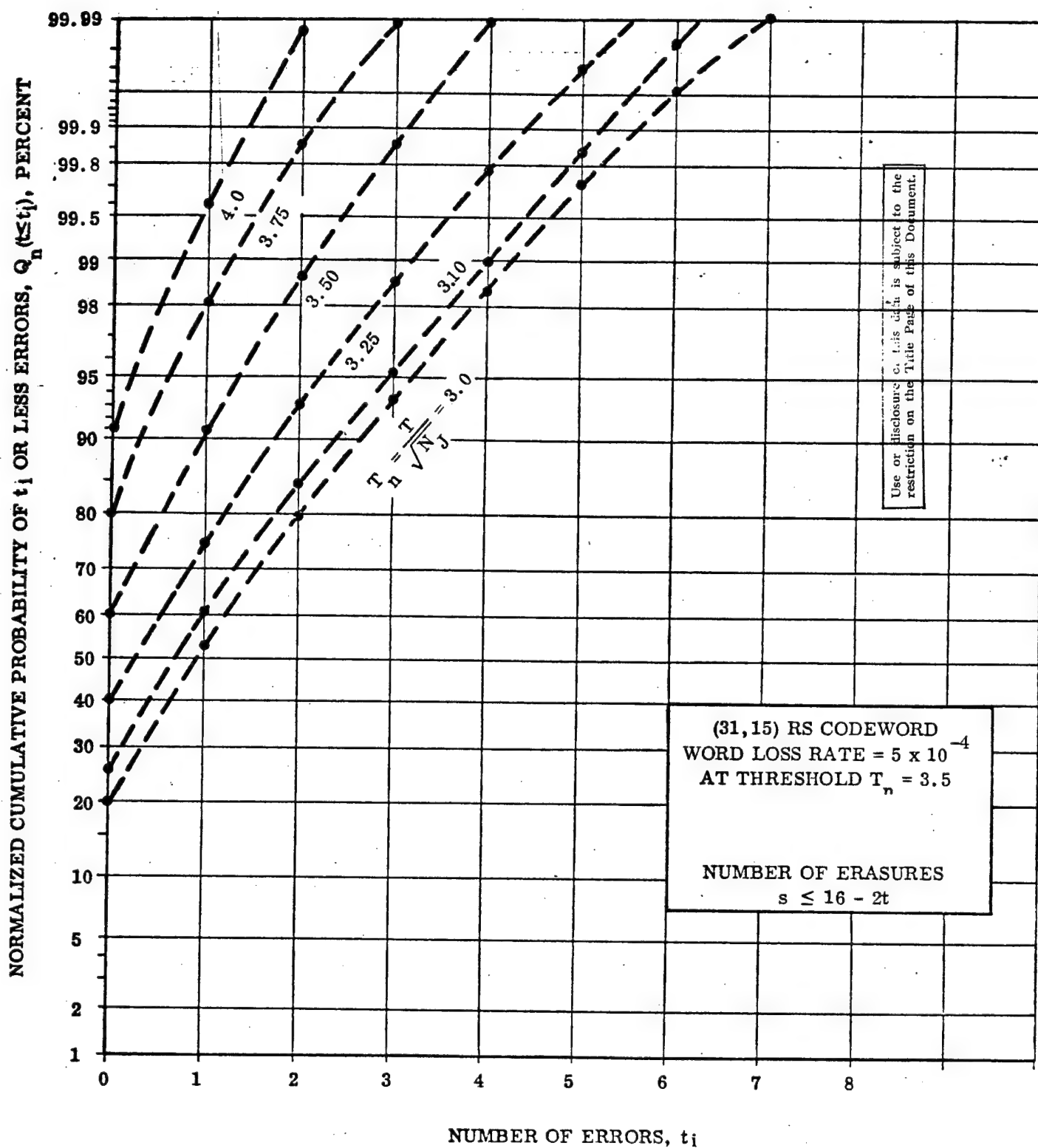


Figure 3. Cumulative Probability of Correctable Errata Patterns

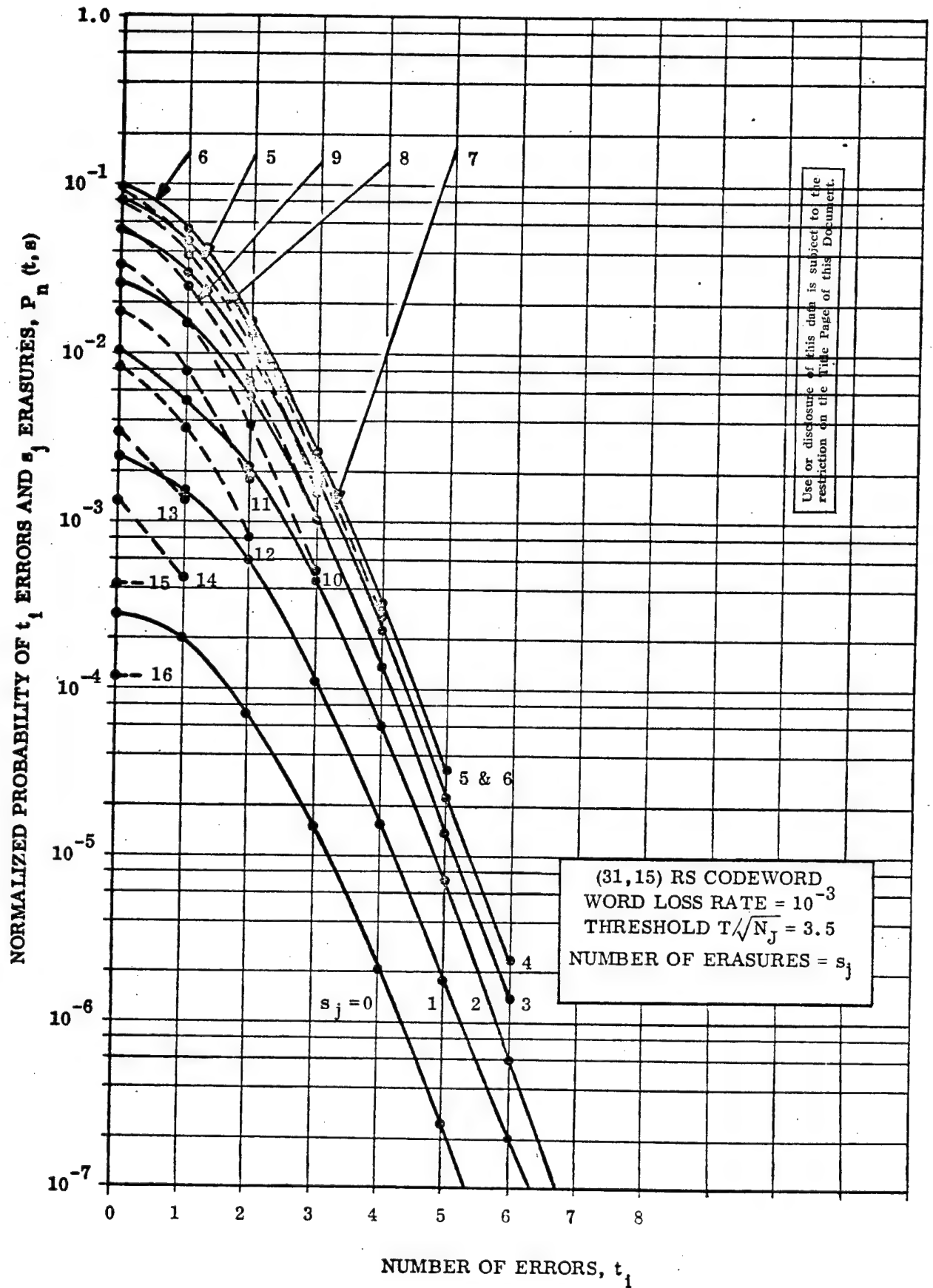


Figure 4. Errata Pattern Probabilities

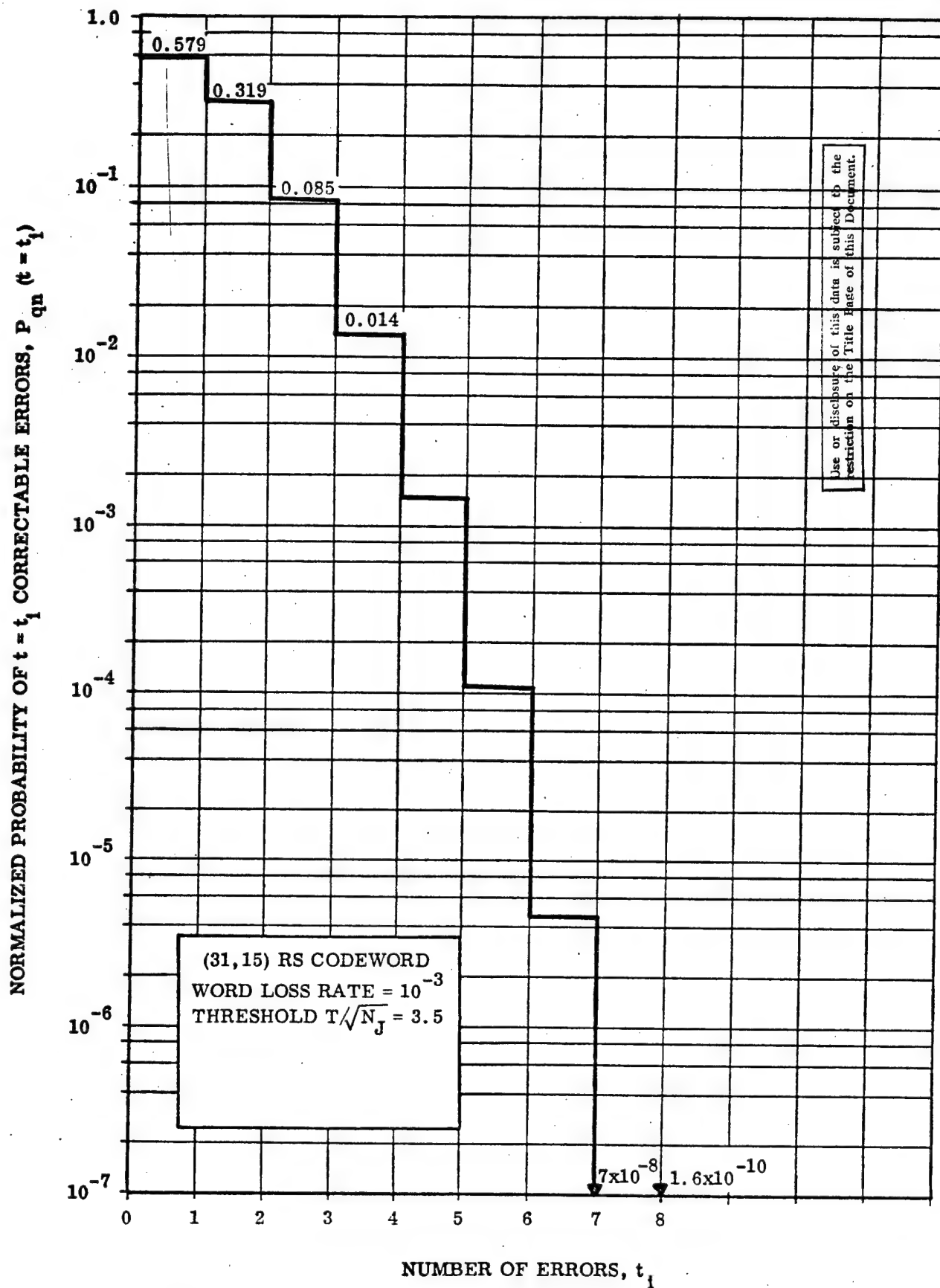


Figure 5. Probability of Correctable Patterns with $t = t_1$ Errors

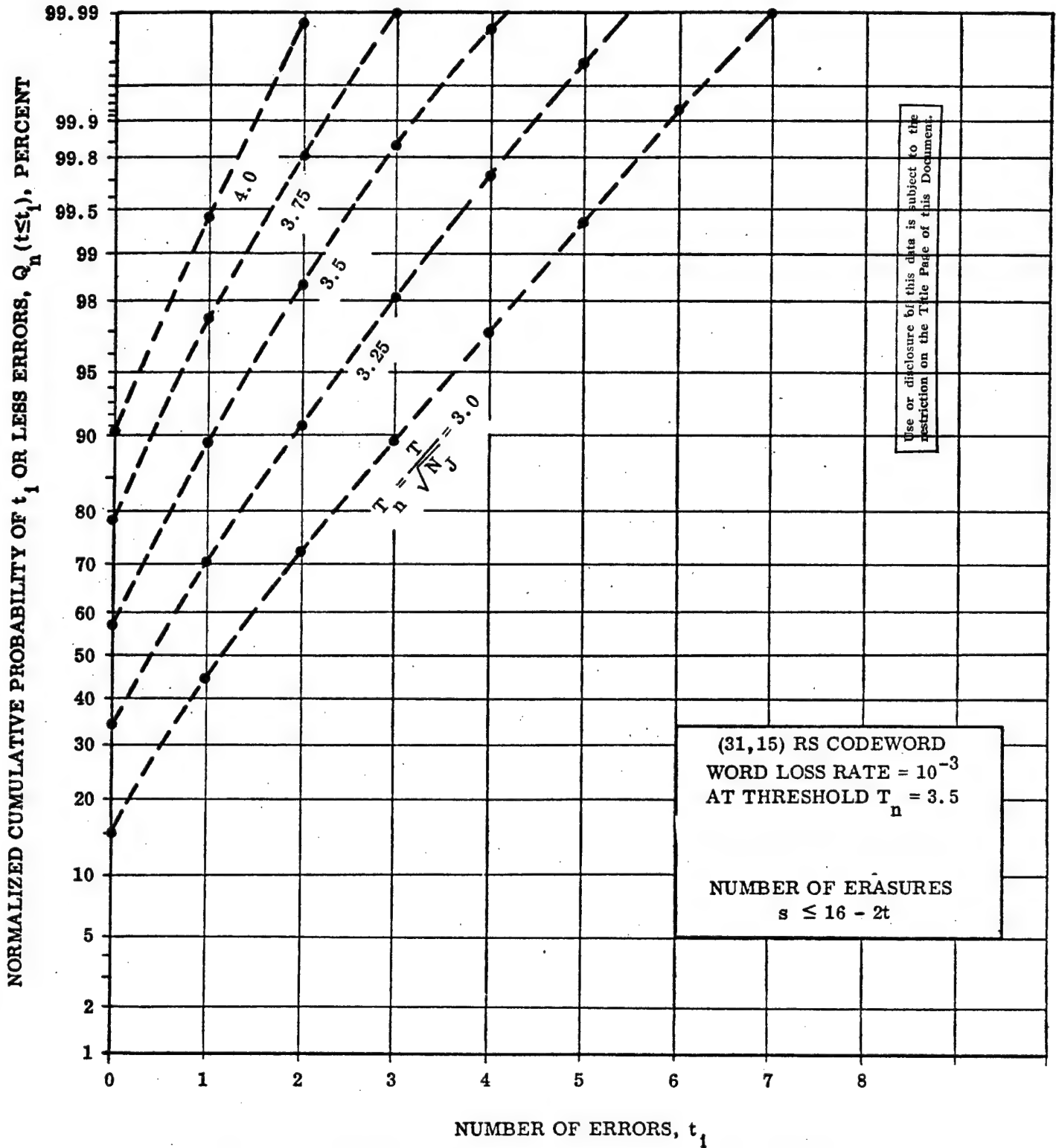


Figure 6. Cumulative Probability of Correctable Errata Patterns

APPENDIX C

PERFORMANCE TEST PROCEDURE
REED SOLOMON ENCODER/DECODER

Prepared for Naval Air Development Center
Under Contract Number N62269-75-C-0503

by

ITT Avionics Division
500 Washington Avenue
Nutley, N. J. 07110

Specification D11723

Sheet 1 of 15

Issue B Date 1/16/76

1. INTRODUCTION

The purpose of these tests is to demonstrate that the Reed-Solomon Encoder/Decoder (RSED) module will satisfy the requirements presented in the RSED Statement of Work. The test data will be presented to the RSED via the User Test Panel. This data is prepared for testing from a pre-defined list of test message patterns. These test messages will include verification of the encoding and decoding processes, RTT recognition and reply, and overall message timing. See Figure 1 for RSED Block Diagram.

2. EQUIPMENT SET-UP

No specific test equipment is required. The Reed Solomon Encoder/Decoder in conjunction with the User Test Panel are sufficient equipment for performing this test procedure. A Tektronix 454 oscilloscope or equivalent is required during those portions of the tests that involve the measurement of timing waveforms.

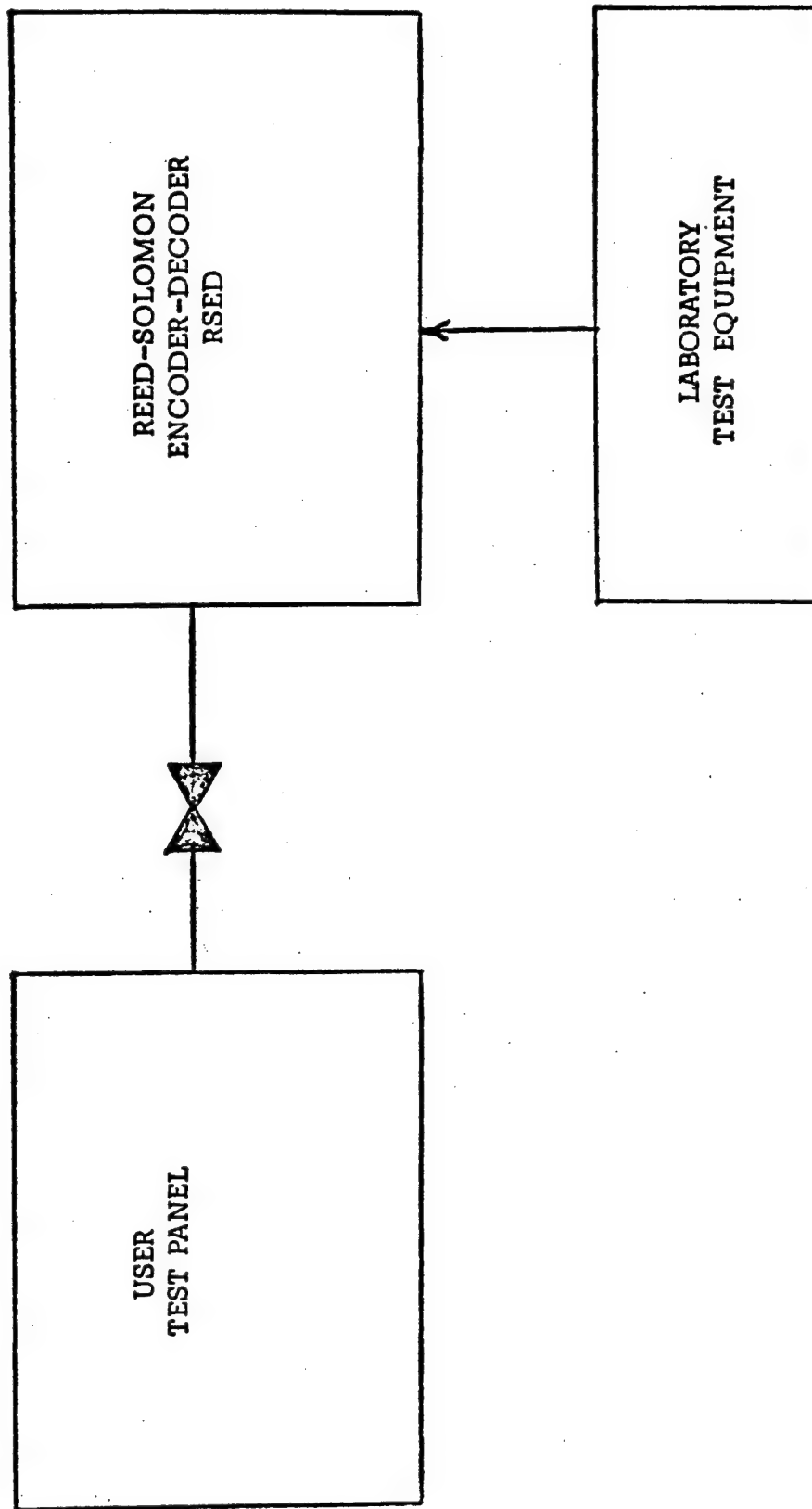
3. PERFORMANCE TESTS

All test data taken for the following tests are to be recorded on the test data sheets supplied. Input test fields are selected at the operator's discretion from data supplied in Appendix A.

3.1 Encoder Tests

3.1.1 Encoder Accuracy

This test will be conducted on a message basis consisting of a Header (4 Data Characters), W1 (15 Data Characters), W2 (15 Data Characters) and W3 (15 Data Characters). Six separate test runs are made using the data presented in the test data sheets 3.1.1.1 thru 3.1.1.6. The "input area" column of the test data sheets represents the input data characters for H, W1, W2 and W3. The "trans word" column represents the correct encoded data characters (data and parity) for H, W1, W2 and W3. The "encoder area" column will be used for entering the data encoded by the RSED hardware and for comparison with the correct data characters to determine encoder accuracy.



RSED BLOCK DIAGRAM

Figure 1

3.1.1.1 Encoder Test Procedure

- A. Set the User test panel switches to the following positions.

<u>Switch</u>	<u>Position</u>
Power	ON
Continuous	OFF
Data-Word	Header
Data-Area	Input
Mode	Encode
Number of Messages	0001

- B. Using data sheets 3.1.1.1 thru 3.1.1.6 (one at a time) manually enter the data characters in the Input Area column. In addition, enter the Xmit data and encoded parities from Appendix A to the "trans word" column. Data characters (in decimal format) are entered by setting the data thumbwheel switches (2) to the desired magnitude and raising the deposit switch. The deposit switch is spring loaded and rests normally in the down position. If a data character greater than 31 is entered on the thumb wheel switches, the data display flashes on and off indicating the insertion of an invalid character.

The position at which data has been entered is displayed. When the advance switch is depressed, the position is advanced to the next position.

- C. After the four Header (H) characters are entered, set the Data-Word switch to W1 and enter 15 W1 data characters.
- D. After the 15 W1 characters are entered set the Data-Word switch to W2 and enter 15 W2 data characters.
- E. After the 15 W2 characters are entered set the Data-Word switch to W3 and enter 15 W3 data characters.
- F. Press the start switch and set the Data-Area switch to Encode and Data-Word switch to Header.

- G. Depressing the advance switch, write down the characters displayed for the Header in the Encoder Area column of the test data sheet. Compare the "Encoder Area" column with the "Trans Word" column and check pass or fail.
- H. Repeat for step G for W1, W2 and W3 by placing Data-Word switch to W1, W2 and W3.

3.1.2 Encoder Timing

This test will be conducted using message blocks consisting of one Header and W1, W2, W3 code words. Enter words as described in paragraph 3.1.1.1.

3.1.2.1 Encoder Timing Test Procedure

- A. Set the User test panel switches to the following positions:

<u>Switch</u>	<u>Position</u>
Number of Messages	0001
Continuous	ON

- B. Press the start switch and observe the following timing waveforms using the Tektronix 475 or equivalent oscilloscope.

Scope Settings

Sync - External +

Mode Triggering - ALT

Vertical Inputs

Channel 1 - Test Point 1, DC

Channel 2 - Test Point 14, DC

Scope GND - Test Point G

Adjust vertical gain for approximately 3 cm. deflection for Ch. 1 and Ch. 2.

Horizontal display - "A" inten
1 ms per cm.

Delayed Sweep - .1 ms/cm

Delayed Time Multiplier - 630

Horiz Display - B Dly'd

Measure time interval between last pos transition of signal on channel 1 to first pos edge transition of signal on channel 2.

Record this measurement on test data sheet for HEADER.
Record the time between pulses on channel 2 for the
time to encode W1, W2, and W3.

3.2 Decoder Tests

3.2.1 Decoder Accuracy and Timing

This test will be conducted on a message block basis to verify the decoding process. Several test words containing the number of errors and erasures (ERRATA) shown in table 1 are presented to the RSED via the User test panel.

3.2.1.1 Decoder Test Procedure

- A. Set the User test panel switches as listed in paragraph 3.1.1.1 (A) and proceed from 3.1.1.1 (A) thru 3.1.1.1 (E) using data sheets 3.2.1.1 thru 3.2.1.5.
- B. Press the start switch and set the Data-Area switch to Errata and Data-Word switch to Header.
- C. Check the displayed characters for the Errata Area column with the Trans Word column.
- D. Repeat step C for W1, W2 and W3 by placing Data-Word switch to W1, W2 and W3.
- E. Insert errors and erasures into the Header, W1, W2 and W3 as per table 1. Errata is entered as follows:

Set Data Area switch to Errata
Set Data Word switch to Header
Set Erasure Switch to OFF

Advance the position to the desired character and insert an error by depositing a character other than the one currently being displayed and write down the new character on the test data sheet under the Inserted Errata column at the present position displayed. Indicate error by "e".

If an erasure is to be inserted, advance the position to the desired character, set character magnitude to zero (00) and insert an erasure by placing the erasure switch on and lifting up the deposit switch. At this point the Red LED labeled erasure will be lit. Indicate erasures by "E".

Enter the position of the inserted erasure in the Errata Area column.

Number of Errors	Number of Erasures (31,15) (16,4)	Number of Erasures (31,15) only
0	0, 4, 8, 12,	13, 16
1	0, 3, 6, 10,	12, 14
2	0, 1, 5, 8,	11, 12
3	0, 3, 5, 6,	7, 10
4	0, 2, 3, 4,	6, 8,
5	0, 1, 2,	4, 6,
6	0	1, 2, 4,
7	-----	0, 1, 2,
8	-----	-----

Table 1. DECODER ACCURACY TEST CASES

- F. Repeat step E for W1, W2 and W3.
- G. Set the mode switch to Decode and recheck that the Number of Messages is set to 0001 and that "Continuous" is set to Off. Press the start switch and set the Data-Area switch to Decoder and Data-Word switch to Header.
- H. Write down the displayed characters by advancing through the decoded data area, for the header in the Decoder Area column. Position 00 displays the number of errors and the decode failure lamp will be lit if a data word was not decoded properly exceeds the error correction capability of the decoder.
- I. Repeat step H for W1, W2 and W3 by placing Data-Word switch to W1, W2 and W3.
- J. The User Test Panel loads the Decoder Data Area 6.7 milliseconds after the start switch is pushed in step G. If the examination of all the decode failure positions for the Header, W1, W2 and W3 results in the decode failure LED not lit, then the decoder corrected the inserted Errata in the time allotted.

Measure the decoder turnaround time using the HP 5345 Counter as follows:

Place continuous switch to On and press the start switch.

Counter Settings

FUNCTION - time int

Gate time/display - 100ms/100ms

Sample Rate - CCW

CHANNEL A

level - preset

Slope - +

Atten - 1 m μ , X 20

AC/DC - AC

COM/SEP - COM A

CHANNEL B

preset

-

1 m μ , X 20

AC

Connect a BNC coax to test point 13 ground to test point G. Record the time displayed in MS on the test data sheet.

- K. Repeat steps A thru J for additional tests as required.

3.2.1.2 Decoder Failure Test Procedure

Repeat steps A thru D of paragraph 3.2.1.1. At step E enter Errata patterns that exceed the power of the decoder. Example 9 errors, 17 erasures, or 4 errors and 9 erasures.

At step H note that the decode failure LED will be lit for the Data Words that have Errata exceeding the power of the decoder.

Measure the decoder turnaround time using the procedure described in paragraph 3.2.1.1. J.

3.3 RTT Tests

3.3.1 RTT Message Recognition Accuracy and Timing

This test is conducted using an RTT Donor Address which is entered into the RTT Input area, RSED encoded, and stored as the RTT Donor Address. A test word is set in the RTT Errata Area which is compared with the RTT Donor Address as shown in table 1 for the (16,4) code.

3.3.1.1 RTT Test Procedure

- A. Set the User test panel switches to the following positions:

<u>Switch</u>	<u>Position</u>
Continuous	OFF
Data-Word	RTT
Data-Area	Input
Mode	Encode
Number of Messages	0001

- B. Using data sheets 3.3.1.1 thru 3.3.1.6 enter manually the data characters in the Input Area column.

- C. Press start switch and set the Data Area to Errata and Data Word to RTT.
- D. Fill In Donor Address column with data from Appendix A.
- E. Check the displayed characters for the Errata Area column with the Donor Address column.
- F. Insert errors and erasures into the RTT Errata Word as per table 1. Errata is entered as described in paragraph 3.2.1.1 E.
- G. Set Mode switch to RTT Trial and Continuous switch to On. Press start switch and measure the following waveforms using the Tektronix 475 oscilloscope.

Scope Setting

Sync - Internal + (Channel 1 only)

Slope - -

Vertical Inputs

Channel 1 - Test Point 5, DC

Channel 2 - Test Point 10, DC

Adjust vertical gain for approximately 3 cm. deflection for ch. 1 and ch. 2.

Mode Trigger - Chop

Sweep Setting

5 microseconds per cm.

Measure the time interval between the negative edge transition of signal on channel 1 to positive edge transition of signal on channel 2.

Note: If no pulse is present on channel 2, the RTT detector may have an Errata pattern entered taht does not exceed the RTT Trial threshold criteria.

- H. If a waveform is present on channel 2, change the scope setting to 100 microsecond per cm., move channel 2 probe to test point 14 and measure the time interval between the negative edge transition of the pulse on channel 1 to the positive transition of the pulse on channel 2.
- I. Repeat steps A thru F for two additional test runs.

3.3.1.2 RTT Address Recognition

This test will demonstrate the ability of the RTT detector to reject messages not addressed to the terminal.

- A. Insert errata from the Appendix A which is unique to the data entered in paragraph 3.3.1.1 or insert errata which exceeds the (16,4) decoder capability.
- B. Proceed to step G of paragraph 3.3.1.1.

3.4 Multifunction RSED Tests

This test will demonstrate the ability of the RSED to perform an encode for Header, W1, W2 and W3, an RTT Trial, RTT Donor Address Outputting, and a decode of a Header W1, W2 and W3 in a 7.8125 msec. time slot.

3.4.1 Test Procedure

- A. Set the User test panel switches to the following positions.

<u>Switch</u>	<u>Position</u>
Continuous	Off
Number of Messages	0001
Mode	Encode
Data-Word	Header
Data-Area	Input

- B. Using data sheets 3.4.1.1 thru 3.4.1.6 enter manually the data characters in the Input Area column for Header, W1, W2 and W3 and RTT.
- C. Press the start switch and set the Data Area switch to Errata and Data Word switch to Header. Insert Errata as per paragraph 3.2.1.1 E (include RTT Errata). Record Errata pattern on test data sheet. Set the mode switch to interleaved.

- D. Set the Continuous switch to On, press the start switch and measure the following waveforms using the Tektronix 475 oscilloscope.

Scope Settings

Sync - Internal - (Channel 1 only)

Vertical Input

Channel 1 - Test Point 12

Sweep Setting

1 millisecond per cm.

Measure the repetition rate of channel 1 waveform and record.

- E. Set Scope as follows for Decoder Input Data

Sync. Ext - Test Point 12

Vertical Input - Alt

Channel 1 - Test Point 5

Channel 2 - Test Point 6

Sweep Setting - 20 usec/cm

X10 magnifier

Measure the number of 400 nanosecond negative transitions on channel 2 for each positive gate on channel 1.

1st gate - Header

2nd gate - W1

3rd gate - W2

4th gate - W3

- F. Set Scope as follows for Decoder Output Data.

Sync. Ext - Test Point 12

Vertical Input - Alt

Channel 1 - Test Point 7

Channel 2 - Test Point 8

Sweep Setting: Main - 1 ms/cm, delayed - 2 usec/cm

Use delaying sweep set at 6.7 msec. and adjust delayed sweep as required.

Measure the number of 400 nanosecond negative transitions on channel 2 for each negative gate on channel 1.

1st gate - Header
2nd gate - W1
3rd gate - W2
4th gate - W3

G. Set Scope as follows for Encoder Input Data.

Sync Ext - Test Point 12

Vertical Input

Channel 1 - Test Point 1

Channel 2 - Test Point 2

Sweep Setting

Use delaying sweep set at approximately 6.6 msec. and adjust delayed sweep as required.

Measure the number of 400 nanosecond negative transitions on channel 2 for each negative gate on channel 1.

1st gate - Header
2nd gate - W1
3rd gate - W2
4th gate - W3

H. Set Scope as follows for Encode Output Data.

Sync Ext - Test Point 12

Vertical Input

Channel 1 - Test Point 3

Channel 2 - Test Point 4

Sweep Setting

Use delaying sweep set approximately 7.6 msec. and adjust delayed sweep as required.

Measure the number of 400 nanosecond negative transitions on channel 2 for each negative gate on channel 1.

1st gate - Header

2nd gate - W1

3rd gate - W2

4th gate - W3

I. Set Scope as follows for RTT Trial.

Sync. Ext - Test Point 12

Vertical Input

Channel 1 - Test Point 5

Channel 2 - Test Point 6

Sweep Setting

Use delaying sweep set at approximately 2 msec. and adjust delayed sweep as required.

Measure the number of 400 nanosecond negative transitions on channel 2 for the negative gate on channel 1.

J. Set Scope as follows for RTT Active.

Sync. Ext - Test Point 12

Vertical Input

Channel 1 - Test Point 5

Channel 2 - Test Point 10

Sweep Setting: main - 1 ms/cm, delayed, 5 usec/cm

Use delaying sweep set at approximately 2 msec and adjust delayed sweep as required.

Measure the time interval from the positive transition of the pulse on channel 1 to the negative transition of the pulse on channel 2.

K. Set Scope as follows for RTT Turnaround Time.

Sync. Ext - Test Point 12

Vertical Input

Channel 1 - Test Point 5

Channel 2 - Test Point 14

Sweep Setting: main - 1 ms/cm, delayed - 50 usec/cm
Use delaying sweep set at approximately
2 msec and adjust delayed sweep as
required.

Measure the time interval from the positive
transition of the pulse on channel 1 to the
negative transition of the pulse on channel 2.

L. Set Scope as follows for Read Out RTT Donor
Address.

Sync. Ext + Test Point 12

Vertical Input

Channel 1 - Test Point 3

Channel 2 - Test Point 4

Sweep Setting

Use delaying sweep set at approximately
2 msec and adjust delayed sweep as
required.

Measure the number of 400 nanosecond negative
transitions on channel 2 for the negative
gate on channel 1.

JTIDS C.S.
REQUEST?

EERUN RESM

JTIDS O.S.
REQUEST?

RUN RESMON

S000
ENCODE

S000
XMIT DATA: . 11 12 13 14

EN PARITY: 12 25 22 05 20 01 25 09 24 08 02 00

S001
XMIT DATA: . 16 10 08 04

EN PARITY: 01 24 08 25 18 25 09 14 16 24 02 29

S002
XMIT DATA: . 19 22 13 24

EN PARITY: 28 17 04 00 03 20 16 15 26 23 27 02

S003
XMIT DATA: . 25 23 08 13

EN PARITY: 09 09 19 15 16 01 17 26 22 29 14 16

S004
XMIT DATA: . 07 23 17 23

EN PARITY: 22 19 24 15 01 05 08 25 09 13 04 31

S005
XMIT DATA: . 25 00 11 13

EN PARITY: 31 25 23 31 12 23 28 12 10 09 12 22

S006
XMIT DATA: . 26 17 06 27

EN PARITY: 01 04 28 03 28 12 30 07 25 26 19 15

Appendix A
Short Code (16,4)

S007

XMIT DATA: . 02 17 12 13

EN PARITY: 14 10 05 07 25 11 15 27 00 24 05 04

S008

XMIT DATA: . 07 03 21 24

EN PARITY: 12 31 03 02 09 26 28 29 11 18 14 16

S009

XMIT DATA: . 25 04 00 29

EN PARITY: 23 15 28 00 12 01 10 04 00 27 11 18

S010

XMIT DATA: . 12 30 10 03

EN PARITY: 12 02 26 04 20 01 00 12 05 10 03 25

S011

XMIT DATA: . 21 02 13 03

EN PARITY: 22 23 30 30 18 00 10 01 03 21 26 24

S012

XMIT DATA: . 28 30 28 04

EN PARITY: 13 18 06 11 19 14 03 11 25 18 21 21

S013

XMIT DATA: . 12 26 30 26

EN PARITY: 24 00 03 13 28 13 28 28 17 15 07 31

S014

XMIT DATA: . 03 12 08 12

EN PARITY: 22 30 23 24 01 22 13 16 20 01 15 20

S015

XMIT DATA: . 23 14 08 08

EN PARITY: 01 28 03 06 06 22 27 20 16 25 18 03

SC16

XMIT DATA: . 06 31 26 05

EN PARITY: 25 22 17 30 23 06 30 26 24 06 03 01

SC17

XMIT DATA: . 07 16 14 07

EN PARITY: 29 26 00 19 15 01 14 06 12 25 23 13

SC18

XMIT DATA: . 02 01 08 01

EN PARITY: 27 11 16 21 30 30 27 04 00 04 04 12

SC19

XMIT DATA: . 15 09 05 24

EN PARITY: 04 05 01 29 02 06 24 00 09 02 14 10

SC20

XMIT DATA: . 31 23 26 31

EN PARITY: 01 19 29 00 26 29 01 01 19 29 11 05

SC21

XMIT DATA: . 13 19 10 13

EN PARITY: 16 22 30 30 19 15 27 22 08 26 25 03

SC22

XMIT DATA: . 28 31 05 01

EN PARITY: 00 25 30 26 27 27 12 16 29 20 00 09

SC23

XMIT DATA: . 20 23 30 18

EN PARITY: 00 30 13 01 06 29 10 06 08 30 01 00

SC24

XMIT DATA: . 18 15 28 25

EN PARITY: 00 23 20 27 16 20 20 21 26 06 04 28

SC25

XMIT DATA: . 06 17 01 08

EN PARITY: 24 31 12 04 01 30 12 23 03 31 23 19

SC26

XMIT DATA: . 03 11 16 00

EN PARITY: 17 28 29 06 16 29 24 14 19 26 23 22

SC27

XMIT DATA: . 26 15 29 02

EN PARITY: 05 20 04 03 13 12 11 22 28 22 18 17

SC28

XMIT DATA: . 31 25 28 04

EN PARITY: 14 16 09 17 08 08 22 00 07 29 12 22

SC29

XMIT DATA: . 09 26 02 19

EN PARITY: 08 05 22 25 19 12 19 19 00 27 09 21

SC30

XMIT DATA: . 10 02 08 03

EN PARITY: 20 29 05 06 07 18 00 18 04 05 26 17

SC31

XMIT DATA: . 30 11 19 29

EN PARITY: 10 20 28 00 22 14 24 14 25 23 30 03

SC32

XMIT DATA: . 30 03 08 19

EN PARITY: 11 22 27 01 22 26 30 00 31 06 12 06

SC33

XMIT DATA: . 12 28 02 05

EN PARITY: 28 03 24 09 01 30 03 21 29 11 25 00

S034

XMIT DATA: . 22 18 11 23

EN PARITY: 30 29 11 03 15 03 21 05 22 29 25 20

S035

XMIT DATA: . 17 24 02 29

EN PARITY: 10 08 23 00 07 01 22 27 04 06 26 25

S036

XMIT DATA: . 03 06 11 02

EN PARITY: 21 21 17 27 22 30 08 04 24 20 05 22

S037

XMIT DATA: . 16 06 08 06

EN PARITY: 24 17 29 27 30 09 11 03 21 02 23 13

S038

XMIT DATA: . 03 00 12 02

EN PARITY: 13 03 06 13 28 06 10 28 18 21 28 24

S039

XMIT DATA: . 04 08 14 26

EN PARITY: 30 23 10 07 10 28 19 16 03 04 17 27

S040

XMIT DATA: . 25 08 28 02

EN PARITY: 05 18 09 16 03 12 27 26 00 29 09 23

S041

XMIT DATA: . 16 07 31 29

EN PARITY: 28 13 07 25 21 04 10 20 12 15 05 22

S042

XMIT DATA: . 03 23 00 20

EN PARITY: 06 27 10 00 28 30 18 23 00 26 12 15

SC43

XMIT DATA: . 28 19 18 07

EN PARITY: 28 25 04 23 01 30 00 28 09 18 07 03

SC44

XMIT DATA: . 31 25 02 07

EN PARITY: 24 06 19 19 15 00 18 30 07 31 04 29

SC45

XMIT DATA: . 10 19 10 23

EN PARITY: 02 15 14 12 17 05 07 12 03 15 31 31

SC46

XMIT DATA: . 28 04 19 04

EN PARITY: 29 00 07 02 10 02 10 10 08 27 16 13

SC47

XMIT DATA: . 07 28 11 28

EN PARITY: 24 19 06 29 30 24 02 22 01 30 27 01

SC48

XMIT DATA: . 06 05 11 11

EN PARITY: 30 10 07 14 14 24 26 01 22 03 15 07

SC49

XMIT DATA: . 14 13 04 09

EN PARITY: 03 24 08 19 06 14 19 04 29 14 07 30

SC50

XMIT DATA: . 16 22 05 16

EN PARITY: 20 04 00 17 27 30 05 14 28 03 06 02

SC51

XMIT DATA: . 25 30 11 30

EN PARITY: 26 12 22 31 19 19 26 23 00 23 23 28

S052

XMIT DATA: . 27 21 09 29

EN PARITY: 23 09 30 20 25 14 29 00 21 25 05 18

S053

XMIT DATA: . 13 06 04 13

EN PARITY: 30 17 20 00 04 20 30 30 17 20 12 09

S054

XMIT DATA: . 02 17 18 02

EN PARITY: 22 24 19 19 17 27 26 24 11 04 03 07

S055

XMIT DATA: . 10 13 09 30

EN PARITY: 00 03 19 04 26 26 28 22 20 01 00 21

S056

XMIT DATA: . 01 06 19 15

EN PARITY: 00 19 02 30 14 20 18 14 11 19 30 00

S057

XMIT DATA: . 15 27 10 03

EN PARITY: 00 06 01 26 22 01 01 31 04 14 23 10

S058

XMIT DATA: . 14 08 30 11

EN PARITY: 29 13 28 23 30 19 28 06 07 13 06 17

S059

XMIT DATA: . 07 12 22 00

EN PARITY: 08 10 20 14 22 20 29 05 17 04 06 24

S060

XMIT DATA: . 04 27 20 25

EN PARITY: 09 01 23 07 02 28 12 24 10 24 15 08

S061

XMIT DATA: . 13 03 10 23

EN PARITY: 05 22 21 08 11 11 24 00 16 20 28 24

S062

XMIT DATA: . 21 04 25 17

EN PARITY: 11 09 24 03 17 28 17 17 00 26 21 31

S063

XMIT DATA: . 18 25 11 07

EN PARITY: 01 20 09 14 16 15 00 15 23 09 04 08

S064

XMIT DATA: . 19 12 17 20

EN PARITY: 18 01 10 00 24 05 29 05 03 06 19 07

S065

XMIT DATA: . 19 07 11 17

EN PARITY: 12 24 26 30 24 04 19 00 13 14 28 14

S066

XMIT DATA: . 28 10 25 09

EN PARITY: 10 07 29 21 30 19 07 31 20 12 03 00

S067

XMIT DATA: . 24 15 12 06

EN PARITY: 19 20 12 07 27 07 31 09 24 20 03 01

S068

XMIT DATA: . 08 29 25 20

EN PARITY: 18 11 06 00 16 30 24 26 23 14 04 03

S069

XMIT DATA: . 07 14 12 25

EN PARITY: 31 31 08 26 24 19 11 23 29 01 09 24

SC70

XMIT DATA: . 22 14 11 14

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JTIDS O.S.
REQUEST?

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L927 XMIT DATA: . 31 23 28 29 10 07 08 02 26 23 25 00 27 30 23
EN PARITY: 03 19 29 08 04 16 06 01 27 17 03 02 13 07 20 11

L928 XMIT DATA: . 08 29 19 06 16 04 17 27 01 13 02 03 11 20 07
EN PARITY: 17 31 18 13 01 17 26 06 12 00 16 26 16 03 27 05

L929 XMIT DATA: . 13 18 31 26 17 01 00 12 06 16 26 16 05 27 03
EN PARITY: 27 07 01 11 25 07 00 26 06 16 09 16 16 20 01 30

L930 XMIT DATA: . 11 01 07 00 07 25 16 06 26 16 16 09 30 01 20
EN PARITY: 00 06 21 19 01 14 26 14 25 06 05 03 08 06 17 10

L931 XMIT DATA: . 19 21 06 26 14 01 06 25 14 08 03 05 10 17 06
EN PARITY: 16 03 03 06 18 11 14 05 03 13 03 27 12 30 01 06

L932 XMIT DATA: . 06 03 03 14 11 18 13 03 05 12 27 03 06 01 30
EN PARITY: 06 09 14 27 04 18 05 11 15 17 31 30 29 30 25 06

L933 XMIT DATA: . 27 14 09 05 18 04 17 15 11 29 30 31 06 25 30
EN PARITY: 02 01 09 21 29 26 00 03 20 19 31 00 03 05 28 00

L934 XMIT DATA: . 21 09 01 00 26 29 19 20 03 03 00 31 00 28 05
EN PARITY: 21 13 24 06 16 30 15 08 28 21 15 20 01 13 22 17

L935 XMIT DATA: . 06 24 13 15 30 16 21 28 08 01 20 15 17 22 13
EN PARITY: 16 17 02 23 30 15 20 30 06 22 15 28 30 20 13 06

L936 XMIT DATA: . 23 02 17 20 15 30 22 06 30 30 28 15 06 13 20
EN PARITY: 31 05 21 18 15 29 31 10 07 27 02 18 29 30 27 00

L937 XMIT DATA: . 18 21 05 31 29 15 27 07 10 29 18 02 00 27 30
EN PARITY: 30 21 27 30 13 20 21 25 28 00 07 01 10 31 22 28

L938 XMIT DATA: . 30 27 21 21 20 13 00 28 25 10 01 07 28 22 31
EN PARITY: 15 19 16 23 21 26 18 25 22 17 04 26 10 07 10 09

L939 XMIT DATA: . 23 16 19 18 26 21 17 22 25 10 26 04 09 10 07
EN PARITY: 07 30 31 07 15 11 06 30 01 10 07 14 20 31 08 02

L940 XMIT DATA: . 07 31 30 06 11 15 10 01 30 20 14 07 02 08 31
EN PARITY: 19 15 13 07 27 26 12 24 19 29 25 30 07 22 19 11

L941 XMIT DATA: . 07 13 15 12 26 27 29 19 24 07 30 25 11 19 22
EN PARITY: 00 07 00 03 05 08 30 23 05 01 26 26 23 13 30 02

L942 XMIT DATA: . 03 00 07 30 08 05 01 05 23 23 26 26 02 30 13
EN PARITY: 28 21 15 29 19 12 12 10 04 06 19 25 04 09 05 31

L943 XMIT DATA: . 29 15 21 12 12 19 06 04 10 04 25 19 31 05 09
EN PARITY: 07 17 02 05 18 31 28 01 10 05 05 14 15 22 03 30

L944 XMIT DATA: . 05 02 17 28 31 18 05 10 01 15 14 05 30 03 22
EN PARITY: 15 06 06 08 17 01 04 02 14 26 14 03 15 31 30 06

L945 XMIT DATA: . 08 06 06 04 01 17 26 14 02 15 03 14 06 30 31
EN PARITY: 10 14 09 09 04 23 13 07 05 26 27 26 00 05 06 18

L946 XMIT DATA: . 09 09 14 13 23 04 26 05 07 00 26 27 18 06 05
EN PARITY: 16 16 29 12 18 12 29 03 10 10 21 12 05 31 17 12

L947 XMIT DATA: . 12 29 16 29 12 18 10 10 03 05 12 21 12 17 31
EN PARITY: 10 02 14 31 13 21 15 30 26 24 30 06 20 08 21 05

L948 XMIT DATA: . 31 14 02 15 21 13 24 26 30 20 06 30 05 21 08
EN PARITY: 26 27 04 06 02 07 30 16 26 19 22 12 10 14 16 07

L949 XMIT DATA: . 06 04 27 30 07 02 19 26 16 10 12 22 07 16 14
EN PARITY: 09 31 10 30 26 19 08 19 13 08 05 05 08 28 15 05

L950 XMIT DATA: . 30 10 31 08 19 26 08 13 19 08 05 05 05 15 28
EN PARITY: 22 30 17 24 15 29 24 31 08 29 00 28 23 03 08 06

L951 XMIT DATA: . 24 17 30 24 29 15 29 08 31 23 28 00 06 08 03
EN PARITY: 17 19 28 19 11 24 19 01 29 05 04 02 01 11 04 21

L952 XMIT DATA: . 19 28 19 19 24 11 05 29 01 01 02 04 21 04 11
EN PARITY: 21 02 13 27 31 10 23 25 19 03 29 13 24 29 08 28

L953 XMIT DATA: . 27 13 02 23 10 31 03 19 25 24 13 29 28 08 29

L954 XMIT DATA: . 26 31 24 19 08 05 20 23 24 19 28 08 05 20 02
EN PARITY: 31 24 18 18 20 01 20 28 01 17 01 07 25 16 29 18

L955 XMIT DATA: . 18 18 24 20 01 20 17 01 28 25 07 01 18 29 16
EN PARITY: 20 00 26 24 13 06 18 13 06 21 23 26 16 20 23 20

L956 XMIT DATA: . 24 26 00 18 06 13 21 06 13 16 26 23 20 23 20
EN PARITY: 13 15 23 27 16 24 29 01 12 30 18 04 04 20 26 06

L957 XMIT DATA: . 27 23 15 29 24 16 30 12 01 04 04 18 06 26 20
EN PARITY: 06 22 30 28 03 06 00 03 29 16 03 28 29 30 16 18

L958 XMIT DATA: . 28 30 22 00 06 03 16 29 03 29 28 03 18 16 30
EN PARITY: 14 10 29 08 00 15 05 02 04 07 21 24 30 03 26 05

L959 XMIT DATA: . 08 29 10 05 15 00 07 04 02 30 24 21 05 26 03
EN PARITY: 29 18 13 12 29 28 06 22 28 27 14 11 27 30 19 27

L960 XMIT DATA: . 12 13 18 06 28 29 27 28 22 27 11 14 27 19 30
EN PARITY: 30 05 05 18 31 06 10 21 16 00 06 06 12 10 02 07

L961 XMIT DATA: . 18 05 05 10 06 31 00 16 21 12 06 06 07 02 10
EN PARITY: 04 17 21 15 10 30 27 09 03 17 01 25 12 08 09 21

L962 XMIT DATA: . 15 21 17 27 30 10 17 03 09 12 25 01 21 09 08
EN PARITY: 29 26 25 18 03 26 23 29 11 11 20 07 06 01 12 19

L963 XMIT DATA: . 18 25 26 23 26 03 11 11 29 06 07 20 19 12 01
EN PARITY: 19 14 16 03 03 19 22 04 27 13 24 31 28 04 07 14

L964 XMIT DATA: . 03 16 14 22 19 03 13 27 04 28 31 24 14 07 04
EN PARITY: 16 10 05 24 13 00 25 24 09 12 02 04 30 17 27 09

L965 XMIT DATA: . 24 05 10 25 00 13 12 09 24 30 04 02 09 27 17
EN PARITY: 24 24 12 17 12 15 01 01 19 08 06 14 10 20 03 07

L966 XMIT DATA: . 17 12 24 01 15 12 08 19 01 10 14 06 07 03 20
EN PARITY: 20 27 14 21 18 29 20 22 03 31 14 21 03 24 18 20

L967 XMIT DATA: . 21 14 27 20 29 18 31 03 22 03 21 14 20 18 24
EN PARITY: 28 29 04 09 29 08 16 15 26 19 12 06 26 31 00 09

L968 XMIT DATA: . 09 04 29 16 08 29 19 26 15 26 06 12 09 00 31
EN PARITY: 15 22 20 28 22 02 12 23 13 24 00 22 17 04 14 24

L969 XMIT DATA: . 28 20 22 12 02 22 24 13 23 17 22 00 24 14 04
EN PARITY: 21 24 01 19 13 23 16 25 16 27 21 17 21 14 03 31

L970 XMIT DATA: . 19 01 24 16 23 13 27 16 25 21 17 21 31 03 14
EN PARITY: 20 29 02 26 31 13 16 16 27 22 05 06 26 25 23 30

L971 XMIT DATA: . 26 02 29 16 13 31 22 27 16 26 06 05 30 23 25
EN PARITY: 28 11 18 17 01 19 03 14 15 18 24 29 14 02 31 08

L972 XMIT DATA: . 17 18 11 03 19 01 18 15 14 14 29 24 08 31 02
EN PARITY: 17 01 11 21 19 09 20 01 07 12 00 06 11 21 21 28

L973 XMIT DATA: . 21 11 01 20 09 19 12 07 01 11 06 00 28 21 21
EN PARITY: 03 03 21 08 30 04 02 17 19 04 31 08 21 26 13 11

L974 XMIT DATA: . 08 21 03 02 04 30 04 19 17 21 08 31 11 13 26
EN PARITY: 14 00 18 11 18 26 05 24 13 14 22 08 29 16 05 27

L975 XMIT DATA: . 11 18 00 05 26 18 14 13 24 29 08 22 27 05 16
EN PARITY: 03 00 19 09 13 00 30 25 26 24 28 09 05 20 14 15

L976 XMIT DATA: . 09 19 00 30 00 13 24 26 25 05 09 28 15 14 20
EN PARITY: 23 16 22 25 09 01 18 24 26 19 29 02 11 16 26 28

L977 XMIT DATA: . 25 22 16 18 01 09 19 26 24 11 02 29 28 26 16
EN PARITY: 13 30 14 01 25 02 21 06 03 25 10 02 11 21 01 28

L978 XMIT DATA: . 01 14 30 21 02 25 25 03 06 11 02 10 28 01 21
EN PARITY: 31 30 02 12 29 30 27 01 30 30 30 28 15 27 27 16

L979 XMIT DATA: . 12 02 30 27 30 29 30 30 01 15 28 30 16 27 27
EN PARITY: 11 27 10 02 24 31 28 22 15 23 29 23 09 07 03 09

L980 XMIT DATA: . 02 10 27 28 31 24 23 15 22 09 23 29 09 03 07
EN PARITY: 18 10 17 27 07 07 16 14 04 17 00 08 18 31 29 19

L981 XMIT DATA: . 27 17 10 16 07 07 17 04 14 18 08 00 19 29 31
EN PARITY: 09 11 30 20 26 13 31 18 19 16 08 03 03 05 10 21

L982 XMIT DATA: . 20 30 11 31 13 26 16 19 18 03 03 08 21 10 05
EN PARITY: 00 13 26 11 21 21 06 22 25 06 27 27 23 01 02 13

L983 XMIT DATA: . 11 26 13 06 21 21 06 25 22 23 27 27 13 02 01
EN PARITY: 30 20 18 03 27 16 07 08 24 02 30 21 13 31 28 10

L984 XMIT DATA: . 03 18 20 07 16 27 02 24 08 13 21 30 10 28 31
EN PARITY: 12 10 26 22 15 09 06 27 08 01 18 03 05 25 31 14

L985 XMIT DATA: . 22 26 10 06 09 15 01 08 27 05 03 18 14 31 25
EN PARITY: 16 02 21 30 13 29 08 22 00 25 19 17 27 17 18 06

L986 XMIT DATA: . 30 21 02 08 29 13 25 00 22 27 17 19 06 18 17
EN PARITY: 10 17 15 03 25 28 02 10 08 11 23 25 06 09 31 29

L987 XMIT DATA: . 03 15 17 02 28 25 11 08 10 06 25 23 29 31 09
EN PARITY: 21 17 15 25 24 30 14 28 24 00 10 05 01 14 09 21

L988 XMIT DATA: . 25 15 17 14 30 24 00 24 28 01 05 10 21 09 14
EN PARITY: 31 13 03 07 07 06 01 23 31 29 03 29 22 30 27 22

L989 XMIT DATA: . 07 03 13 01 06 07 29 31 23 22 29 03 22 27 30
EN PARITY: 28 29 13 07 18 20 24 29 01 17 28 19 13 25 31 30

L990 XMIT DATA: . 07 13 29 24 20 18 17 01 29 13 19 28 30 31 25
EN PARITY: 02 04 23 24 10 06 00 03 24 10 08 20 16 27 24 22

L991 XMIT DATA: . 24 23 04 00 06 10 10 24 03 16 20 08 22 24 27
EN PARITY: 26 13 18 16 07 30 25 00 11 15 11 03 19 29 14 16

L992 XMIT DATA: . 16 18 13 25 30 07 15 11 00 19 03 11 16 14 29
EN PARITY: 19 06 13 28 25 15 18 19 07 01 11 09 01 29 19 01

L993 XMIT DATA: . 28 13 06 18 15 25 01 07 19 01 09 11 01 19 29
EN PARITY: 04 16 09 23 27 23 08 23 12 20 11 31 20 31 17 22

L994 XMIT DATA: . 23 09 16 08 23 27 20 12 23 20 31 11 22 17 31
EN PARITY: 28 13 20 02 27 04 19 05 18 19 01 18 20 22 22 04

L995 XMIT DATA: . 02 20 13 19 04 27 19 18 05 20 18 01 04 22 22
EN PARITY: 23 03 07 04 03 12 00 05 02 04 14 15 27 03 08 27

L996 XMIT DATA: . 04 07 03 00 12 03 04 02 05 27 15 14 27 08 03
EN PARITY: 09 17 08 12 04 20 06 31 27 30 30 00 14 15 10 22

L997 XMIT DATA: . 12 08 17 06 20 04 30 27 31 14 00 30 22 10 15
EN PARITY: 07 31 26 06 12 26 01 05 31 15 11 01 01 24 04 09

L998 XMIT DATA: . 06 26 31 01 26 12 15 31 05 01 01 11 09 04 24
EN PARITY: 04 25 04 15 18 08 01 15 06 22 23 14 17 00 02 29

JTIDS O.S.
REQUEST?

APPENDIX D

TEST DATA SHEETS

REED SOLOMON ENCODER/DECODER

Prepared for Naval Air Development Center
Under Contract Number N62269-75-C-0503

by

ITT Avionics Division
500 Washington Avenue
Nutley, N.J. 07110

Test Performed By: Michael Ferraro ITTAV

Test Witnessed By: Valerie J. Quinn

Test Performed
1/19/1976

Data Sheets

Issue B Date 1/16/76

Sheet ___ of ___

D11724

RSED Test Data Sheet

Test Encoder Accuracy Par. 3.1.1.1-1

A P

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
H S 808	01	10	10	10	✓	
	02 } Data	04	04	04	✓	
	03	11	11	11	✓	
	04	15	15	15	✓	
	05		14	14	✓	
	06		31	31	✓	
	07		22	22	✓	
	08 } Parity		07	07	✓	
	09		28	28	✓	
	10		10	10	✓	
	11		07	07	✓	
	12		11	11	✓	
	13		13	13	✓	
	14		10	10	✓	
	15		05	05	✓	
	16		03	03	✓	

Test Encoder Accuracy Par. 3.1.1. 1 - 2

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
W1 L011	01	20	20	20	✓	
	02	09	09	09	✓	
	03	07	07	07	✓	
	04 } Data	22	22	22	✓	
	05	20	20	20	✓	
	06	24	24	24	✓	
	07	22	22	22	✓	
	08	28	28	28	✓	
	09	04	04	04	✓	
	10	20	20	20	✓	
	11	11	11	11	✓	
	12	27	27	27	✓	
	13	12	12	12	✓	
	14	12	12	12	✓	
	15	16	16	16	✓	
	16		22	22	✓	
	17		07	07	✓	
	18		30	30	✓	
	19		31	31	✓	
	20		04	04	✓	
	21 } Parity		17	17	✓	
	22		07	07	✓	
	23		14	14	✓	
	24		15	15	✓	
	25		10	10	✓	
	26		05	05	✓	
	27		19	19	✓	
	28		17	17	✓	
	29		29	29	✓	
	30		16	16	✓	
	31		20	20	✓	

Test Encoder Accuracy Par. 3.1.1. 1-3

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
W2 L 098	01	04	04	04		
	02	26	26	26	✓	
	03	19	19	19	✓	
	04 } Data	13	13	13	✓	
	05	29	29	29	✓	
	06	28	28	28	✓	
	07	04	04	04	✓	
	08	01	01	01	✓	
	09	06	06	06	✓	
	10	02	02	02	✓	
	11	03	03	03	✓	
	12	07	07	07	✓	
	13	24	24	24	✓	
	14	00	00	00	✓	
	15	27	27	27	✓	
	16		31	31	✓	
	17		03	03	✓	
	18		27	27	✓	
	19		02	02	✓	
	20		21	21	✓	
	21 } Parity		04	04	✓	
	22		19	19	✓	
	23		04	04	✓	
	24		08	08	✓	
	25		20	20	✓	
	26		27	27	✓	
	27		21	21	✓	
	28		18	18	✓	
	29		14	14	✓	
	30		09	09	✓	
	31		00	00	✓	

Test Encoder Accuracy Par. 3.1.1. 1-4

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
W3 L174	01	22	22	22	✓	
	02	12	12	12		
	03	00	00	00		
	04	Data 31	31	31		
	05	29	29	29		
	06	20	20	20		
	07	16	16	16		
	08	31	31	31		
	09	03	03	03		
	10	19	19	19		
	11	18	18	18		
	12	18	18	18		
	13	13	13	13		
	14	04	04	04		
	15	10	10	10		
	16		28	28		
	17		14	14		
	18		30	30		
	19		22	22		
	20		10	10		
	21	Parity	00	00		
	22		01	01		
	23		26	26		
	24		07	07		
	25		31	31		
	26		06	06		
	27		27	27		
	28		29	29		
	29		26	26		
	30		20	20		
	31		01	01	✓	

RSED Test Data Sheet

Test Encoder Accuracy Par. 3.1.1.2-1

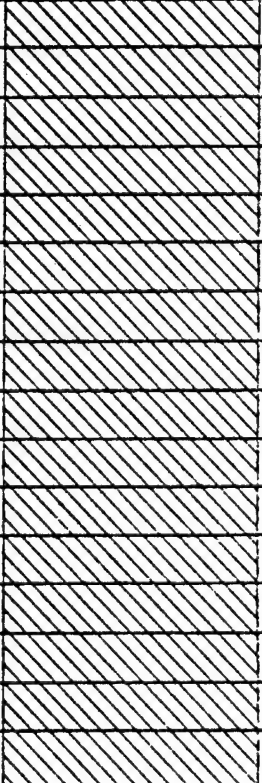
A P

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
H S224	01	20	20	20	✓	
	02 } Data	27	27	27		
	03	30	30	30		
	04	00	00	00		
	05		18	18		
	06		04	04		
	07		08	08		
	08 Parity		13	13		
	09		30	30		
	10		08	08		
	11		17	17		
	12		02	02		
	13		10	10		
	14		09	09		
	15		31	31	✓	
	16		19	19		

Test Encoder Accuracy Par. 3.1.1. 2-2

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
<u>W1</u>						
<u>L 156</u>	01	19	19	19	✓	
	02	16	16	16		
	03	08	08	08		
	04 Data	18	18	18		
	05	23	23	23		
	06	24	24	24		
	07	06	06	06		
	08	00	00	00		
	09	11	11	11		
	10	16	16	16		
	11	22	22	22		
	12	00	00	00		
	13	00	00	00		
	14	16	16	16		
	15	22	22	24		
	16		04	04		
	17		01	01		
	18		10	10		
	19		14	14		
	20		10	10		
	21 Parity		10	10		
	22		25	26		
	23		28	28		
	24		04	04		
	25		01	01		
	26		15	15		
	27		23	23		
	28		09	09		
	29		24	24		
	30		06	06		
	31		22	22		

Test Encoder Accuracy Par. 3.1.1. 2-3

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
<u>W2</u> <u>L181</u>	01	01	01	01	✓	
	02	28	28	28		
	03	10	10	10		
	04 } Data	02	02	02		
	05	16	16	16		
	06	06	06	06		
	07	04	04	04		
	08	27	27	27		
	09	07	07	07		
	10	16	16	16		
	11	10	10	10		
	12	11	11	11		
	13	11	11	11		
	14	01	01	01		
	15	20	20	20		
	16		26	26		
	17		15	15		
	18		25	25		
	19		07	07		
	20		03	03		
	21 } Parity		29	29		
	22		22	22		
	23		17	17		
	24		08	08		
	25		28	28		
	26		26	26		
	27		20	20		
	28		25	25		
	29		08	08		
	30		07	07		
	31		10	10		

Test Encoder Accuracy

Par. 3.1.1.

2-4

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
W3 1172	01	22	22	22	✓	
	02	20	20	20		
	03	06	06	06		
	04	Data 15	15	15		
	05	02	02	02		
	06	09	09	09		
	07	06	06	06		
	08	02	02	02		
	09	26	26	26		
	10	06	06	06		
	11	30	30	30		
	12	17	17	17		
	13	07	07	07		
	14	25	25	26		
	15	04	04	04		
	16		05	05		
	17		11	11		
	18		24	24		
	19		09	09		
	20		15	15		
	21	Parity	02	02		
	22		13	13		
	23		20	20		
	24		11	11		
	25		30	30		
	26		03	03		
	27		14	14		
	28		18	18		
	29		25	25		
	30		02	02		
	31		06	06		

RSED Test Data Sheet

Test Encoder Accuracy Par. 3.1.1.3-1

NT2

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
# 5619	01	19	19	19	✓	
	02 } Data	13	13	13		
	03	09	09	09		
	04	02	02	02		
	05		06	06		
	06		28	28		
	07		03	03		
	08 } Parity		01	01		
	09		09	09		
	10		21	21		
	11		03	03		
	12		30	30		
	13		27	27		
	14		28	28		
	15		30	30	↓	
	16		31	31		

Test Encoder Accuracy Par. 3.1.1. 3-2

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
L14 W-1	01	02	02	02	✓	
	02	25	25	25		
	03	12	12	12		
	04 Data	23	23	23		
	05	20	20	20		
	06	12	12	12		
	07	22	22	22		
	08	26	26	26		
	09	31	31	31		
	10	03	03	03		
	11	20	20	20		
	12	09	09	09		
	13	18	18	18		
	14	25	25	25		
	15	23	23	23		
	16		22	22		
	17		05	05		
	18		11	11		
	19		31	31		
	20		31	31		
	21 Parity		24	24		
	22		10	10		
	23		25	25		
	24		08	08		
	25		27	27		
	26		31	31		
	27		16	16		
	28		01	01		
	29		00	00		
	30		19	19		
	31		29	29		

Test Encoder Accuracy Par. 3.1.1. 3-3

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
<u>W2</u> <u>2084</u>	01	31	31	31	✓	
	02	16	16	16		
	03	06	06	06		
	04	Data 28	28	28		
	05	31	31	31		
	06	13	13	13		
	07	00	00	00		
	08	18	18	18		
	09	21	21	21		
	10	28	28	28		
	11	27	27	27		
	12	08	08	08		
	13	08	08	08		
	14	05	05	05		
	15	18	18	18		
	16		16	16		
	17		26	26		
	18		01	01		
	19		14	14		
	20		27	27		
	21	Parity	06	06		
	22		15	15		
	23		21	21		
	24		22	22		
	25		10	10		
	26		24	24		
	27		01	01		
	28		19	19		
	29		08	08		
	30		31	31		
	31		28	28	✓	

Test Encoder Accuracy

Par. 3.1.1.3-4

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
10-3	01	20	20	20	✓	
1342	02	26	26	26		
	03	13	13	13		
	04 Data	07	07	07		
	05	05	05	05		
	06	18	18	18		
	07	19	19	19		
	08	03	03	03		
	09	21	21	21		
	10	22	22	22		
	11	18	18	18		
	12	00	00	00		
	13	28	28	28		
	14	05	05	05		
	15	13	13	13		
	16		05	05		
	17		30	30		
	18		26	26		
	19		13	13		
	20		12	12		
	21 Parity		26	26		
	22		12	12		
	23		05	05		
	24		15	15		
	25		17	17		
	26		23	23		
	27		14	14		
	28		02	02		
	29		02	02		
	30		06	06		
	31		23	23	✓	

RSED Test Data Sheet

Test Encoder Accuracy Par. 3.1.1.4-1

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
H S006	01	26	26	26		
	02 } Data	17	17	17		
	03	06	06	06		
	04	27	27	27		
	05		01	01		
	06		04	04		
	07		28	28		
	08 } Parity		03	03		
	09		28	28		
	10		12	12		
	11		30	30		
	12		07	07		
	13		25	25		
	14		26	26		
	15		19	19		
	16		15	15		

Test Encoder Accuracy Par. 3.1.1. 4-2

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
W1 — L514	01	16	16	16		
	02	00	00	00		
	03	16	16	16		
	04 } Data	00	00	00		
	05	25	25	25		
	06	23	23	23		
	07	28	28	28		
	08	30	30	30		
	09	06	06	06		
	10	20	20	20		
	11	19	19	19		
	12	03	03	03		
	13	25	25	25		
	14	19	19	19		
	15	08	08	08		
	16		12	12		
	17		19	19		
	18		13	13		
	19		30	30		
	20		04	04		
	21 } Parity		10	10		
	22		04	04		
	23		17	17		
	24		10	10		
	25		18	18		
	26		00	00		
	27		13	13		
	28		17	17		
	29		14	14		
	30		26	26		
	31		20	20		

Test Encoder Accuracy Par. 3.1.1. 4 - 3

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
W2 — 4652	01	15	15	15		
	02	05	05	05		
	03	13	13	13		
	04 } Data	31	31	31		
	05	15	15	15		
	06	18	18	18		
	07	00	00	00		
	08	06	06	06		
	09	06	06	06		
	10	09	09	09		
	11	09	09	09		
	12	06	06	06		
	13	29	29	29		
	14	28	28	28		
	15	25	25	25		
	16		09	09		
	17		31	31		
	18		10	10		
	19		11	11		
	20		03	03		
	21 } Parity		21	21		
	22		11	11		
	23		25	25		
	24		19	19		
	25		04	04		
	26		27	27		
	27		04	04		
	28		22	22		
	29		08	08		
	30		04	04		
	31		29	29		

Test Encoder Accuracy Par. 3.1.1. 4 - 4

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
W3 L348	01	27	27	27		
	02	21	21	21		
	03	02	02	02		
	04 } Data	08	08	08		
	05	13	13	13		
	06	29	29	29		
	07	26	26	26		
	08	31	31	31		
	09	20	20	20		
	10	16	16	16		
	11	30	30	30		
	12	27	27	27		
	13	10	10	10		
	14	02	02	02		
	15	12	12	12		
	16		09	09		
	17		00	00		
	18		24	24		
	19		17	17		
	20		09	09		
	21 } Parity		30	30		
	22		26	26		
	23		14	14		
	24		22	22		
	25		15	15		
	26		31	31		
	27		26	26		
	28		28	28		
	29		21	21		
	30		02	02		
	31		13	13		

RSED Test Data Sheet

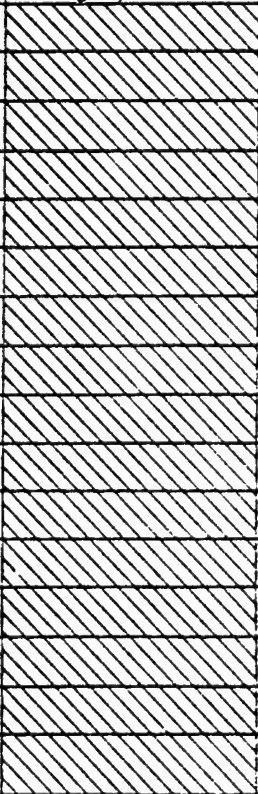
Test Encoder Accuracy Par. 3.1.1.5-1

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
# 3012	01	28	28	28		
	02 } Data	30	30	30		
	03	28	28	28		
	04	04	04	04		
	05		13	13		
	06		18	18		
	07		06	06		
	08 } Parity		11	11		
	09		19	19		
	10		14	14		
	11		03	03		
	12		11	11		
	13		25	25		
	14		18	18		
	15		21	21		
	16		21	21		

Test Encoder Accuracy Par. 3.1.1. 5-2

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
W-1 L727	01	02	02	02		
	02	09	09	09		
	03	10	10	10		
	04 } Data	26	26	26		
	05	18	18	18		
	06	06	06	06		
	07	23	23	23		
	08	16	16	16		
	09	22	22	22		
	10	13	13	13		
	11	17	17	17		
	12	16	16	16		
	13	01	01	01		
	14	03	03	03		
	15	05	05	05		
	16		20	20		
	17		07	07		
	18		22	22		
	19		04	04		
	20		03	03		
	21 } Parity		25	25		
	22		18	18		
	23		14	14		
	24		16	16		
	25		03	03		
	26		06	06		
	27		08	08		
	28		21	21		
	29		18	18		
	30		18	18		
	31		07	07		

Test Encoder Accuracy Par. 3.1.1. 5-3

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
<u>W-2</u> <u>L031</u>	01	17	17	17		
	02	01	01	01		
	03	24	24	24		
	04 } Data	17	17	17		
	05	10	10	10		
	06	09	09	09		
	07	20	20	20		
	08	17	17	17		
	09	06	06	06		
	10	19	19	19		
	11	11	11	11		
	12	05	05	05		
	13	01	01	01		
	14	10	10	10		
	15	07	07	07		
	16		15	15		
	17		14	14		
	18		09	09		
	19		13	13		
	20		11	11		
	21 } Parity		03	03		
	22		30	30		
	23		09	09		
	24		18	18		
	25		28	28		
	26		20	20		
	27		01	01		
	28		13	13		
	29		30	30		
	30		21	21		
	31		28	28		

Test Encoder Accuracy

Par. 3.1.1. 5-4

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
<u>W-3</u> <u>1270</u>	01	14	14	14		
	02	09	09	09		
	03	03	03	03		
	04 } Data	14	14	14		
	05	16	16	16		
	06	03	03	03		
	07	31	31	31		
	08	15	15	15		
	09	06	06	06		
	10	04	04	04		
	11	16	16	16		
	12	28	28	28		
	13	20	20	20		
	14	05	05	05		
	15	01	01	01		
	16		03	03		
	17		25	25		
	18		10	10		
	19		29	29		
	20		17	17		
	21 } Parity		05	05		
	22		10	10		
	23		02	02		
	24		06	06		
	25		21	21		
	26		26	26		
	27		30	30		
	28		17	17		
	29		11	11		
	30		31	31		
	31		27	27		

RSED Test Data Sheet

Test Encoder Accuracy Par. 3.1.1.6-1

ATP

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
H S-415	01	02	02	02	✓	
	02 } Data	20	20	20		
	03	29	29	29		
	04	18	18	18		
	05		07	07		
	06		29	29		
	07		26	26		
	08 Parity		15	16		
	09		17	17		
	10		22	22		
	11		18	18		
	12		00	00		
	13		20	20		
	14		17	17		
	15		24	24		
	16		31	31	✓	

Test Encoder Accuracy Par. 3.1.1.6-2

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
W-1	01	27	27	27	✓	
L-146	02	23	23	23		
	03	21	21	21		
	04	Data 17	17	17		
	05	13	13	13		
	06	08	08	08		
	07	20	20	20		
	08	30	30	30		
	09	03	03	03		
	10	18	18	18		
	11	00	00	00		
	12	15	16	15		
	13	12	12	12		
	14	17	17	17		
	15	21	21	21		
	16		02	02		
	17		04	04		
	18		28	28		
	19		16	16		
	20		29	29		
	21	Parity	10	10		
	22		14	14		
	23		01	01		
	24		07	07		
	25		06	06		
	26		11	11		
	27		19	19		
	28		00	00		
	29		04	04		
	30		24	24		
	31		13	13	✓	

Test Encoder Accuracy Par. 3.1.1. 6-3

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
<u>W-2</u>	01	13	13	13	✓	
<u>L-32</u>	02	09	09	09		
	03	14	14	14		
	04 } Data	30	30	30		
	05	13	03	03		
	06	11	11	11		
	07	28	28	28		
	08	18	18	18		
	09	09	09	09		
	10	13	13	13		
	11	01	01	01		
	12	20	20	20		
	13	28	28	28		
	14	21	21	21		
	15	30	30	30		
	16		23	23		
	17		18	18		
	18		27	27		
	19		05	05		
	20		11	11		
	21 } Parity		15	15		
	22		03	03		
	23		15	15		
	24		22	22		
	25		09	09		
	26		31	31		
	27		28	28		
	28		30	30		
	29		09	09		
	30		00	00		
	31		02	02	✓	

Test Encoder Accuracy Par. 3.1.1.6-4

WORD	POSITION	INPUT AREA	TRANS WORD	ENCODER AREA	RESULTS	
					PASS	FAIL
W.3 L-641	01	07	07	07	✓	
	02	27	27	27		
	03	13	13	13		
	04 Data	27	27	27		
	05	23	23	23		
	06	18	18	18		
	07	15	15	15		
	08	13	13	13		
	09	28	28	28		
	10	22	22	22		
	11	27	27	27		
	12	20	20	20		
	13	01	01	01		
	14	16	16	16		
	15	28	28	28		
	16		13	13		
	17		07	07		
	18		21	21		
	19		05	05		
	20		02	02		
	21 Par. ty		10	10		
	22		01	01		
	23		07	07		
	24		24	24		
	25		03	03		
	26		13	13		
	27		10	10		
	28		24	24		
	29		01	01		
	30		19	19		
	31		23	23	✓	

RSED Test Data Sheet

Encoder Timing

Par. 3.1.2

Header 120

Allowed 300 microseconds max.

W1 240

Allowed 300 microseconds max.

W2 240

Allowed 300 microseconds max.

W3 240

Allowed 300 microseconds max.

RS232 Test Data Sheet

Test Decoder Accuracy

Par. 3.2.1. L-1

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
# Header 3016	05 (Qual)					00		
	01	06	06	06	06			
	02	31	31	31	31			
	03	26	26	26	26			
	04	05	05	05	05			
	05		25	25	25			
	06		22	22	22			
	07	Parity	17	17	17			
	08		30	30	30			
	09		23	23	23			
	10		06	06	06			
	11		30	30	30			
	12		26	26	26			
	13		24	24	24			
	14		06	06	06			
	15		03	03	03			
	16		01	01	01			

Test Summary: Number of Errors 0 Pass Fail

Number of Erasures 0

Measured Time

Test Decoder Accuracy Par. 3.2.1. 1-2

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
W1 L123	16 (Qual)					00		
	01	12	12	12	12			
	02	22	22	22	00E			
	03	15	15	15	15			
	04	28	28	28	00E			
	05 Data	21	21	21	21			
	06	01	01	01	01			
	07	25	25	25	25			
	08	29	29	29	29			
	09	02	02	02	02			
	10	28	28	28	28			
	11	18	18	18	18			
	12	29	29	29	29			
	13	21	21	21	21			
	14	03	03	03	00E			
	15	28	28	28	28			
	16		26	26	26			
	17		10	10	10			
	18		05	05	05			
	19 Parity		06	06	06			
	20		03	03	03			
	21		07	07	07			
	22		12	12	12			
	23		31	31	31			
	24		17	17	17			
	25		22	22	22			
	26		19	19	19			
	27		00	00	00			
	28		11	11	11			
	29		30	30	30			
	30		28	28	00E			
	31		19	19	19			

Test Summary: Number of Errors 0 Pass Fail
Number of Erasures 4

Test Decoder Accuracy Par. 3.2.1. 1-3

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
<u>W2</u> L998	16 (Qual)					00		
	01	06	06	06	06			
	02	26	26	26	26			
	03	31	31	31	31			
	04	01	01	01	01			
	05 Data	26	26	26	00E			
	06	12	12	12	12			
	07	15	15	15	15			
	08	31	31	31	31			
	09	05	05	05	05			
	10	01	01	01	00E			
	11	01	01	01	00E			
	12	11	11	11	00E			
	13	09	09	09	00E			
	14	04	04	04	00E			
	15	24	24	24	24			
	16		04	04	04			
	17		25	25	25			
	18		04	04	04			
	19 Parity		15	15	15			
	20		18	18	00E			
	21		08	08	00E			
	22		01	01	01			
	23		15	15	15			
	24		06	06	06			
	25		22	22	22			
	26		23	23	23			
	27		14	14	14			
	28		17	17	17			
	29		00	00	00			
	30		02	02	02			
	31		29	29	29			

Test Summary: Number of Errors 0 Pass Fail
 Number of Erasures 8

Test Decoder Accuracy Par. 3.2.1.1-4

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
W3 L669	16 (Qual)					00		
	01	31	31	31	00E			
	02	06	06	06	00E			
	03	29	29	29	00E			
	04	13	13	13	00E			
	05 Data	15	15	15	00E			
	06	29	29	29	00E			
	07	31	31	31	00E			
	08	14	14	14	14			
	09	11	11	11	11			
	10	04	04	04	04			
	11	04	04	04	04			
	12	25	25	25	25			
	13	02	02	02	02			
	14	11	11	11	11			
	15	28	28	28	00E			
	16		12	12	00E			
	17		25	25	00E			
	18		20	20	20			
	19 Parity		08	08	08			
	20		30	30	00E			
	21		10	10	00E			
	22		30	30	00E			
	23		10	10	00E			
	24		17	17	17			
	25		13	13	13			
	26		02	02	02			
	27		19	19	19			
	28		11	11	00E			
	29		27	27	00E			
	30		20	20	20			
	31		00	00	00			

Test Summary: Number of Errors 0 Pass Fail
Number of Erasures 16

RSED Test Data Sheet

Test Decoder Accuracy

Par. 3.2.1.2-1

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
H Header S335	05 (Qual)					01		
	01	19	19	19	19			
	02 Data	00	00	00	00			
	03	06	06	06	012			
	04	01	01	01	01			
	05		20	20	20			
	06		19	19	19			
	07 Parity		03	03	03			
	08		20	20	20			
	09		14	14	14			
	10		03	03	03			
	11		05	05	05			
	12		14	14	14			
	13		09	09	09			
	14		24	24	24			
	15		14	14	14			
	16		12	12	12			

Test Summary: Number of Errors 1 Pass Fail

Number of Erasures 0

Measured Time

Test Decoder Accuracy Par. 3.2.1. 2-2

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
<u>W1</u> L383	16 (Qual)					02		
	01	26	26	26	26			
	02	22	22	22	00 E			
	03	29	29	29	29			
	04	05	05	05	05			
	05 Data	15	15	15	00 E			
	06	24	24	24	24			
	07	16	16	16	16			
	08	31	31	31	00 E			
	09	22	22	22	22			
	10	04	04	04	04			
	11	18	18	18	21 e			
	12	14	14	14	14			
	13	01	01	01	01			
	14	28	28	28	28			
	15	01	01	01	01			
	16		13	13	13			
	17		17	17	00 E			
	18		08	08	08			
	19 Parity		19	19	19			
	20		11	11	11			
	21		26	26	26			
	22		27	27	27			
	23		11	11	11			
	24		10	10	00 E			
	25		11	11	11			
	26		19	19	19			
	27		16	16	16			
	28		15	15	15			
	29		09	09	09			
	30		21	21	21			
	31		04	04	07 e			

Test Summary: Number of Errors 2 Pass Fail
Number of Erasures 5

Test Decoder Accuracy Par. 3.2.1. 2-3

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
W2 L781	16 (Qual)					04		
	01	06	06	06	06			
	02	22	22	22	11 e			
	03	27	27	27	27			
	04	04	04	04	04			
	05 Data	29	29	29	06 e			
	06	15	15	15	15			
	07	09	09	09	00 E			
	08	28	28	28	28			
	09	31	31	31	31			
	10	10	10	10	00 E			
	11	01	01	01	01			
	12	09	09	09	09			
	13	21	21	21	21			
	14	20	20	20	17 e			
	15	14	14	14	14			
	16		06	06	00 E			
	17		09	09	09			
	18		28	28	28			
	19 Parity		27	27	00 E			
	20		17	17	17			
	21		01	01	00 E			
	22		29	29	29			
	23		01	01	01			
	24		15	15	00 E			
	25		31	31	31			
	26		06	06	06			
	27		09	09	25 e			
	28		06	06	06			
	29		21	21	00 E			
	30		25	25	25			
	31		20	20	00 E			

Test Summary: Number of Errors 4 Pass Fail
Number of Erasures 8

Test Decoder Accuracy Par. 3.2.1. 2-4

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
<u>W3</u>	16 (Qual)					03		
L782	01	27	27	27	13 e			
	02	28	28	28	28			
	03	09	09	09	00 E			
	04	29	29	29	29			
	05 Data	01	01	01	00 E			
	06	17	17	17	17			
	07	31	31	31	00 E			
	08	15	15	15	15			
	09	01	01	01	01			
	10	06	06	06	00 E			
	11	09	09	09	09			
	12	06	06	06	15 e			
	13	20	20	20	20			
	14	25	25	25	25			
	15	21	21	21	04 e			
	16		15	15	15			
	17		29	29	00 E			
	18		11	11	11			
	19 Parity		01	01	00 E			
	20		22	22	22			
	21		15	15	00 E			
	22		16	16	16			
	23		13	13	13			
	24		16	16	16			
	25		13	13	00 E			
	26		20	20	00 E			
	27		00	00	00			
	28		18	18	18			
	29		17	17	17			
	30		05	05	00 E			
	31		21	21	21			

Test Summary: Number of Errors 3 Pass Fail
Number of Erasures 10

RSED Test Data Sheet

Test Decoder Accuracy

Par. 3.2.1 2-1

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
Header S106	05 (Qual)					05		
	01	07	07	07	03e			
	02 } Data	12	12	12	12			
	03	18	18	18	18			
	04	03	03	03	03			
	05		21	21	15e			
	06		27	27	27			
	07 } Parity		31	31	31			
	08		24	24	19e			
	09		16	16	16			
	10		10	10	07e			
	11		04	04	04			
	12		23	23	23			
	13		00	00	00			
	14		01	01	01			
	15		31	31	31			
	16		14	14	05e			

Test Summary: Number of Errors 5 Pass Fail

Number of Erasures 0

Measured Time

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
W-1	16 (Qual)					06		
1051	01	23	23	23	23			
	02	03	03	03	03			
	03	05	05	05	05			
	04	27	27	27	15e			
	05 Data	01	01	01	01			
	06	20	20	20	20			
	07	31	31	31	31			
	08	25	25	25	25			
	09	27	27	27	27			
	10	06	06	06	03e			
	11	15	15	15	09e			
	12	27	27	27	27			
	13	05	05	05	05			
	14	09	09	09	09			
	15	22	22	22	17e			
	16		08	08	08			
	17		31	31	31			
	18		22	22	22			
	19 Parity		20	20	20			
	20		29	29	22e			
	21		12	12	12			
	22		06	06	06			
	23		23	23	11e			
	24		15	15	15			
	25		13	13	00E			
	26		01	01	01			
	27		30	30	30			
	28		28	28	00E			
	29		28	28	28			
	30		05	05	05			
	31		05	05	05			

Test Summary: Number of Errors 6 Pass Fail
 Number of Erasures 2

Test Decoder Accuracy Par. 3.2.1. 3-3

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
W-2 L897	16 (Qual)					05		
	01	25	25	25	07e			
	02	11	11	11	11			
	03	02	02	02	02			
	04	01	01	01	01			
	05 Data	22	22	22	22			
	06	30	30	30	01e			
	07	25	25	25	25			
	08	22	22	22	22			
	09	14	14	14	00E			
	10	29	29	29	29			
	11	21	21	21	21			
	12	27	27	27	27			
	13	08	08	08	08			
	14	22	22	22	14e			
	15	00	00	00	00			
	16		09	09	09			
	17		31	31	00E			
	18		21	21	21			
	19 Parity		09	09	00E			
	20		23	23	23			
	21		09	09	09			
	22		04	04	00E			
	23		16	16	16			
	24		18	18	18			
	25		27	27	19e			
	26		28	28	12e			
	27		19	19	19			
	28		22	22	00E			
	29		24	24	00E			
	30		14	14	14			
	31		00	00	00			

Test Summary: Number of Errors 5 Pass Fail
 Number of Erasures 6

Test Decoder Accuracy

Par. 3.2.1

3-4

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
W3 1273	16 (Qual)					08		
	01	04	04	04	04			
	02	08	08	08	02e			
	03	04	04	04	04			
	04	22	22	22	22			
	05 Data	13	13	13	07e			
	06	10	10	10	10			
	07	14	14	14	14			
	08	16	16	16	13e			
	09	10	10	10	10			
	10	19	19	19	19			
	11	17	17	17	17			
	12	06	06	06	06			
	13	23	23	23	11e			
	14	31	31	31	31			
	15	14	14	14	14			
	16		03	03	03			
	17		01	01	01			
	18		07	07	07			
	19 Parity		07	07	01e			
	20		09	09	09			
	21		01	01	01			
	22		08	08	08			
	23		28	28	28			
	24		30	30	21e			
	25		17	17	17			
	26		21	21	12e			
	27		19	19	19			
	28		01	01	01			
	29		22	22	22			
	30		17	17	17e			
	31		06	06	06			

Test Summary: Number of Errors 8 Pass Fail
 Number of Erasures 0

MSD Test Data Sheet

ATP

Test Decoder Accuracy

Par. 3.2.1. —

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
Header S415	05 (Qual)					05	✓	
	01	02	02	02	13	02	✓	
	02 } Data	20	20	20	20	20	✓	
	03	29	29	29	29	29	✓	
	04	18	18	18	10	18	✓	
	05		07	07	22			
	06		29	29	29			
	07 } Parity		26	26	26			
	08		15	15	15			
	09		17	17	17			
	10		22	22	27			
	11		18	18	18			
	12		00	00	00			
	13		20	20	20			
	14		17	17	16			
	15		24	24	24			
	16		31	31	31			

Test Summary: Number of Errors 5 Pass ✓ Fail —

Number of Erasures 0

Measured Time 3.061 ms

Test Decoder Accuracy Par. 3.2.1. _____

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
W-1 L-146	16 (Qual)					06	✓	
	01	27	27	27	27	27		
	02	23	23	23	23	23		
	03	21	21	21	21	21		
	04	17	17	17	17	17		
	05 Data	13	13	13	13	13		
	06	08	08	08	08	08		
	07	26	20	20	20	20		
	08	30	30	30	30	30		
	09	03	03	03	03	03		
	10	18	18	18	18	18		
	11	00	00	00	00	00		
	12	15	15	15	15	15		
	13	12	12	12	12	12		
	14	17	17	17	17	17		
	15	21	21	21	21	21	✓	
	16		22	02	02			
	17		04	04	04			
	18		28	28	28			
	19 Parity		16	16	16			
	20		29	29	29			
	21		10	10	10			
	22		14	14	14			
	23		01	01	01			
	24		07	07	07			
	25		06	06	06			
	26		11	11	02 e			
	27		19	19	02 e			
	28		00	00	02 e			
	29		04	04	02 e			
	30		24	24	02 e			
	31		13	13	02 e			

Test Summary: Number of Errors 6 Pass ☒ Fail ☐
 Number of Erasures 0

Test Decoder Accuracy Par. 3.2.1. _____

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
W-2 L-032	16 (Qual)					09	✓	
	01	13		13	13	13		
	02	09		09	09	09		
	03	14		14	14	14		
	04	30		30	30	30		
	05 Data	03		8	03	03		
	06	11		11	11	11		
	07	28		26	28	28		
	08	18		18	18	18		
	09	09		09	15e	09		
	10	13		13	27e	13		
	11	01		01	03e	01		
	12	20		20	06e	20		
	13	28		28	27e	28		
	14	21		21	14e	21		
	15	30		30	16e	30	✓	
	16			23	23			
	17			18	18			
	18			27	27			
	19 Parity			05	05			
	20			11	11			
	21			15	15			
	22			03	03			
	23			15	15			
	24			22	22			
	25			09	09			
	26			31	31			
	27			28	28			
	28			30	30			
	29			09	09			
	30			00	00			
	31			02	02			

Test Summary: Number of Errors 7 Pass ✓ Fail
 Number of Erasures 0

Test Decoder Accuracy Par. 3.2.1. _____

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
W3 L-641	16 (Qual)					08	✓	
	01	07		07	07	07		
	02	27		27	27	27		
	03	13		13	23e	13		
	04	27		29	29	29		
	05 Data	23		23	23	23		
	06	18		18	18	18		
	07	15		15	27e	15		
	08	13		13	13	13		
	09	28		28	28	28		
	10	22		22	22	22		
	11	27		27	15e	27		
	12	20		20	20	20		
	13	01		01	01	01		
	14	16		16	16	16		
	15	28		28	00e	28	✓	
	16			13	13			
	17			07	07			
	18			21	21			
	19 Parity			05	01e			
	20			02	02			
	21			10	10			
	22			01	01			
	23			07	30e			
	24			24	24			
	25			03	03			
	26			13	13			
	27			10	28e			
	28			24	24			
	29			01	01			
	30			19	19			
	31			23	28e			

Test Summary: Number of Errors 8 Pass ✓ Fail
 Number of Erasures 0

3.061/2

Trail own 455

ATP

RSED Test Data Sheet

Test Decoder Accuracy
Par. 3.2.1. 4-1

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
Header S-415	05 (Qual)					06	✓	
	01	01		02	23e	02	↓	
	02	20		20	10e	20	↓	
	03	29		29	13e	29	↓	
	04	18		18	18	18	↓	
	05			07	07			
	06			29	29			
	07			26	26			
	08			15	15			
	09			17	17			
	10			22	22			
	11			18	18			
	12			00	00			
	13			20	20			
	14			17	20e			
	15			24	00e			
	16			31	01e			

Test Summary: Number of Errors 6 Pass ✓ Fail
Number of Erasures 0
Measured Time 3.748ms

Worst case tested 4.149

Test Decoder Accuracy Par. 3.2.1. 4-2

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
W1 L146	16 (Qual)							
	01	27		27 15	27	27 04		
	02	23		23 15	23	23		
	03	21		21 15	21	21		
	04	17		17 15	17	17		
	05 Data	13		13 15	13	13		
	06	08		08	08	08		
	07	20		20	20	20		
	08	30		30	00 E	30 02		
	09	03		03	00 E	03 02		
	10	18		18	00 E	18 02		
	11	00		00	00 E	00 02		
	12	15		15	00 E	15 02		
	13	12		12	00 E	12 02		
	14	17		17	00 E	17 02		
	15	21		21	00 E	21 02		
	16			02	00 E			
	17			04	00 E			
	18			28	00 E			
	19 Parity			16	00 E			
	20			29	00 E			
	21			10	00 E			
	22			14	00 E			
	23			01	00 E			
	24			07	07			
	25			06	06			
	26			11	11			
	27			19	19			
	28			00	00			
	29			04	04			
	30			24	24			
	31			13	13			

Test Summary: Number of Errors 1 Pass 16 Fail 0
 Number of Erasures 16

1.66 sec - 4.166 words - 1.336 MB

- 1) First test 16 Erasures - passed decode
- 2) Second test 16 " + 1 error - detected failure (coded word - KSED did not)
- 3) Third " " " 2 errors - Same as above test (2)

Test Decoder Accuracy Par. 3.2.1. 4-3

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
W2 L632	16 (Qual)					08	✓	
	01	13		13	16e	03		
	02	09		09	16e	09		
	03	14		14	16e	14		
	04	30		30	16e	30		
	05 Data	03		03	02 16e	03		
	06	11		11	11	11		
	07	28		28	28	28		
	08	18		18	18	18		
	09	09		09	09	09		
	10	13		13	13	13		
	11	01		01	01	01		
	12	20		20	20	20		
	13	28		28	28	28		
	14	21		21	21	21		
	15	30		30	30	30		
	16			23	23			
	17			18	18			
	18			27	27			
	19 Parity			05	05			
	20			11	11			
	21			15	15			
	22			03	03			
	23			15	15			
	24			22	22			
	25			09	09			
	26			31	31			
	27			28	28			
	28			30	30			
	29			09	26e			
	30			00	26e			
	31			02	26e			

Test Summary: Number of Errors 8 Pass ✓ Fail
 Number of Erasures 0

Test Decoder Accuracy

Par. 3.2.1. 4-4

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
W3 L-641	16 (Qual)					08		
	01	07		07	17e	07		
	02	27		27	17e	27		
	03	13		13	17e	13		
	04	29		29	17e	29		
	05 Data	23		23	17e	23		
	06	18		18		18		
	07	15		15		15		
	08	13		13		13		
	09	28		28		28		
	10	22		22		22		
	11	27		27		27		
	12	20		20		20		
	13	01		01		01		
	14	16		16		16		
	15	28		28		28		
	16			13				
	17			07				
	18			21				
	19 Parity			05				
	20			02				
	21			10				
	22			01				
	23			07				
	24			24				
	25			03				
	26			13				
	27			10				
	28			24				
	29			01	27e			
	30			17	27e			
	31			23	27e			

Test Summary: Number of Errors 8 Pass ☒ Fail ☐
 Number of Erasures 0

Time H-W3: 3.748ms

RSED Test Data Sheet

Test Decoder Accuracy

Par. 3.2.1. 5-1

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
H Header S 335	05 (Qual)					16		
	01	19	19	19	032			
	02 Data	00	00	00	00E			
	03	06	06	06	192			
	04	01	01	01	252			
	05		20	20	20			
	06		19	19	00E			
	07 Parity		03	03	03			
	08		20	20	00E			
	09		14	14	14			
	10		03	03	03			
	11		05	05	00E			
	12		14	14	14			
	13		09	09	00E			
	14		24	24	112			
	15		14	14	14			
	16		12	12	12			

Test Summary: Number of Errors 5 Pass Fail

Number of Erasures 10

Measured Time

Test Decoder Accuracy Par. 3.2.1. 5-2

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
<u>W1</u> L383	16 (Qual)					16		
	01	26	26	26	11 2			
	02	22	22	22	22			
	03	29	29	29	00 E			
	04	05	05	05	05			
	05 Data	15	15	15	17 2			
	06	24	24	24	24			
	07	16	16	16	00 E			
	08	31	31	31	00 E			
	09	22	22	22	22			
	10	04	04	04	20 2			
	11	18	18	18	00 E			
	12	14	14	14	14			
	13	01	01	01	00 E			
	14	28	28	28	28			
	15	01	01	01	30 2			
	16		13	13	13			
	17		17	17	00 E			
	18		08	08	00 E			
	19 Parity		19	19	19			
	20		11	11	00 E			
	21		26	26	26			
	22		27	27	27			
	23		11	11	00 E			
	24		10	10	10			
	25		11	11	00 E			
	26		19	19	19			
	27		16	16	00 E			
	28		15	15	15 2			
	29		09	09	09			
	30		21	21	00 E			
	31		04	04	07 2			

Test Summary: Number of Errors 0 Pass Fail
 Number of Erasures 12

Test Decoder Accuracy

Par. 3.2.1. 5-3

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
<u>W2</u>	16 (Qual)					16		
<u>L781</u>	01	06	06	06	06			
	02	22	22	22	11 e			
	03	27	27	27	27			
	04	04	04	04	04			
	05 Data	29	29	29	06 e			
	06	15	15	15	15			
	07	09	09	09	00 E			
	08	28	28	28	28			
	09	31	31	31	31			
	10	10	10	10	00 E			
	11	01	01	01	01			
	12	09	09	09	21 e			
	13	21	21	21	21			
	14	20	20	20	17 e			
	15	14	14	14	14			
	16		06	06	00 E			
	17		09	09	09			
	18		28	28	28			
	19 Parity		27	27	00 E			
	20		17	17	17			
	21		01	01	00 E			
	22		29	29	29			
	23		01	01	01			
	24		15	15	00 E			
	25		31	31	31			
	26		06	06	06			
	27		09	09	25 e			
	28		06	06	06			
	29		21	21	00 E			
	30		25	25	25			
	31		20	20	00 E			

Test Summary: Number of Errors 5 Pass Fail
 Number of Erasures 8

Test Decoder Accuracy

Par. 3.2.1.

5-4

WORD	POSITION	INPUT AREA	TRANS WORD	ERRATA AREA	INSERTED ERRATA	DECODER AREA	RESULTS	
							PASS	FAIL
<u>W3</u>	16 (Qual)					16		
L782	01	27	27	27	13 e			
	02	28	28	28	28			
	03	09	09	09	00 E			
	04	29	29	29	29			
	05 Data	01	01	01	00 E			
	06	17	17	17	17			
	07	31	31	31	00 E			
	08	15	15	15	15			
	09	01	01	01	25 e			
	10	06	06	06	00 E			
	11	09	09	09	09			
	12	06	06	06	15 e			
	13	20	20	20	20			
	14	25	25	25	25			
	15	21	21	21	04 e			
	16		15	15	15			
	17		29	29	00 E			
	18		11	11	11			
	19 Parity		01	01	00 E			
	20		22	22	22			
	21		15	15	00 E			
	22		16	16	16			
	23		13	13	13			
	24		16	16	00 E			
	25		13	13	00 E			
	26		20	20	20			
	27		00	00	00			
	28		18	18	00 E			
	29		17	17	17			
	30		05	05	00 E			
	31		21	21	21			

Test Summary: Number of Errors 4 Pass Fail
 Number of Erasures 11

RSED Test Data Sheet

Test RTT Tests

Par. 3.3.1.1. - 1

WORD	POSITION	INPUT AREA	RTT DONOR ADDRESS	ERRATA AREA	INSERTED ERRATA	RTT RECOGNITION FLAG
RTT 5855	01	19	19	19	00e	Allowed Time: 75 microsec. max. Measured Time: <u>16.90</u> microsec. Pass <input checked="" type="checkbox"/> Fail <input type="checkbox"/>
	02 Data	14	14	14	14	
	03	29	29	29	20e	
	04	09	09	09	18e	
	05		03	03	03	RTT Processing Time Allowed Time: 375 microsec. max. Measured Time: <u>230</u> microsec. Pass <input checked="" type="checkbox"/> Fail <input type="checkbox"/>
	06		25	25	00E	
	07		27	27	00E	
	08		18	18	00E	
	09		21	21	21	
	10		17	17	17	
	11		00	00	00	
	12		17	17	00E	
	13		28	28	28	
	14		27	27	00E	
	15		12	12	12	
	16		24	24	00E	

RSED Test Data Sheet

ATP

Test RTT Tests

Par. 3.3.1.1. - 2

WORD	POSITION	INPUT AREA	RTT DONOR ADDRESS	ERRATA AREA	INSERTED ERRATA	RTT RECOGNITION FLAG
RTT S492	01	02	02	02	02	Allowed Time: 75 microsec. max.
	02 Data	11	11	11	11	Measured Time: 17.5 microsec.
	03	09	09	09	09	Pass <input checked="" type="checkbox"/> Fail <input type="checkbox"/>
	04	28	28	28	28	RTT Processing Time
	05		04	04	11e	Allowed Time: 375 microsec. max.
	06		26	26	26	Measured Time: 240 microsec.
	07		01	01	13e	Pass <input checked="" type="checkbox"/> Fail <input type="checkbox"/>
	08		29	29	30e	
	09		10	10	10	
	10		25	25	25	
	11		00	00	02e	
	12		25	25	25	
	13		22	22	22	
	14		01	01	02e	
	15		16	16	17e	
	16		05	05	05	

RSED Test Data Sheet

Test RTT Tests

Par. 3.3.1.1.-3

WORD	POSITION	INPUT AREA	RTT DONOR ADDRESS	ERRATA AREA	INSERTED ERRATA	RTT RECOGNITION FLAG
RTT S---	01					Allowed Time: 75 microsec. max.
	02 Data					
	03					Measured Time: ____ microsec.
	04					Pass ____ Fail ____
	05					RTT Processing Time
	06					
	07					Allowed Time: 375 microsec. max.
	08					Measured Time: ____ microsec.
	09					Pass ____ Fail ____
	10					
	11					
	12					
	13					
	14					
	15					
	16					

RSED Test Data Sheet

ATP

Test RTT Address Recognition

Par. 3.3.1.2.-1

WORD	POSITION	INPUT AREA	RTT DONOR ADDRESS	ERRATA AREA	RTT RECOGNITION FLAG
RTT S961	01	25	25	24e	No Flag Present <input checked="" type="checkbox"/>
	02	26	26	04e	Flag Present <input type="checkbox"/>
	03	30	30	00e	
	04	26	26	12e	Pass <input checked="" type="checkbox"/> Fail <input type="checkbox"/>
	05		07	31e ⁽¹⁾	
	06		01	29e	
	07		16	20e	
	08		10	11e	
	09		29	29	
	10		06	06	
	11		19	19	
	12		13	13	
	13		14	14	
	14		21	21	
	15		27	27	
	16		09	09	

NOTE: No flag should be present during this test.

RSED Test Data Sheet

ATP

Test RTT Address Recognition

Par. 3.3.1.2.-2

WORD	POSITION	INPUT AREA	RTT DONOR ADDRESS	ERRATA AREA	RTT RECOGNITION FLAG
RTT S035	01	17	17	00E	No Flag Present <input checked="" type="checkbox"/> Flag Present _____ Pass <input checked="" type="checkbox"/> Fail _____
	02	24	24	00E	
	03	02	02	00E	
	04	29	29	00E	
	05		10	00E	NOTE: No flag should be present during this test.
	06		08	00E	
	07		23	00E	
	08		00	00E	
	09		07	00E	
	10		01	00E	
	11		22	00E	
	12		27	00E	
	13		04	04	
	14		06	06	
	15		26	00E	
	16		25	00E	

RSMD Test Data Sheet

Test RTT Address Recognition

Par. 3.3.1.2.-3

WORD	POSITION	INPUT AREA	RTT DONOR ADDRESS	ERRATA AREA	RTT RECOGNITION FLAG
RTT S195	01	04	04	07e	No Flag Present _____
	02	22	22	03e	Flag Present _____
	03	18	18		
	04	29	29	(10)e	Pass _____ Fail _____
	05		08		
	06		17		
	07		02		
	08		31		
	09		20		
	10		23	00E	
	11		00		
	12		23	00E	
	13		54	00E	
	14		02	22e	
	15		05	10e	
	16		10		

NOTE: No flag should be present during this test.

ATP

RSED Test Data Sheet

Multifunction RSED Tests

Par. 3.4.1

3.4.1(D) Slot Time

Measured Time 7.8127 milliseconds

Allowed Time 7.8125 msec \pm 1%

3.4.1(E) Decoder Input Data

Header

Measured Transitions	<u>16</u>
Allowed	<u>16</u>

W1

Measured Transitions	<u>31</u>
Allowed	<u>31</u>

W2

Measured Transitions	<u>31</u>
Allowed	<u>31</u>

W3

Measured Transitions	<u>31</u>
Allowed	<u>31</u>

3.4.1(F) Decoder Output Data

Header

Measured Transitions	<u>4</u>
Allowed	<u>4</u>

W1

Measured Transitions	<u>15</u>
Allowed	<u>15</u>

W2

Measured Transitions
Allowed

15
15

W3

Measured Transitions
Allowed

15
15

3.4.1(G) Encoder Input Data

Header

Measured Transitions
Allowed

4
4

W1

Measured Transitions
Allowed.

15
15

OK

W2

Measured Transitions
Allowed

15
15

W3

Measured Transitions
Allowed

15
15

3.4.1(H) Encode Output Data

Header

Measured Transitions
Allowed

16
16

W1

Measured Transitions
Allowed

31
31

W2

Measured Transitions
Allowed

31
31

W3

Measured Transitions

31

Allowed

31

3.4.1(I) RTT Trial

Measured Transitions

16

Allowed

16

3.4.1(J) RTT Active

Measured Time

17

microseconds

Allowed

75 microsec. max.

3.4.1(K) RTT Turnaround Time

Measured Time

230

microseconds

Allowed Time

375 microsec. max.

3.4.1(L) Read Out RTT

Measured Transitions

16

Allowed

16

APPENDIX E

RSED ACCEPTANCE TEST PLAN

Prepared Under Contract N62269-75-C-0503

For

Department of the Navy, Naval Air Development Center

By: ITT Avionics Division
500 Washington Avenue
Nutley, New Jersey 07110

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I. INTRODUCTION

The purpose of these tests is to demonstrate that the Reed-Solomon Encoder/Decoder (RSED) module will satisfy the requirements presented in the Statement of Work. These requirements are discussed in Section II. The test data will be presented to the RSED via the User Test Panel and provide for testing from a prior prepared list of test message patterns. These test messages will include verification of the encoding and decoding processes RTT recognition and reply and overall message timing. See Figure 1 for RSED Block Diagram.

II. REED-SOLOMON MODULE REQUIREMENTS

1.0 Encoder

1.1 Short Code

The encoder will accept twenty information bits grouped into four characters (5 bits each) and encode them into a (16,4) Reed-Solomon word consisting of the four original characters and twelve additional parity check characters. The time to encode the word shall not exceed 300 usec.

1.2 Standard Code

The encoder will accept seventy-five information bits grouped into fifteen characters (5 bits each) and encode them into a (31,15) Reed-Solomon word consisting of the fifteen original characters and sixteen additional parity check characters. The time to encode the word shall not exceed 300 usec.

Figure 2 shows the form required of the encoding algorithm.

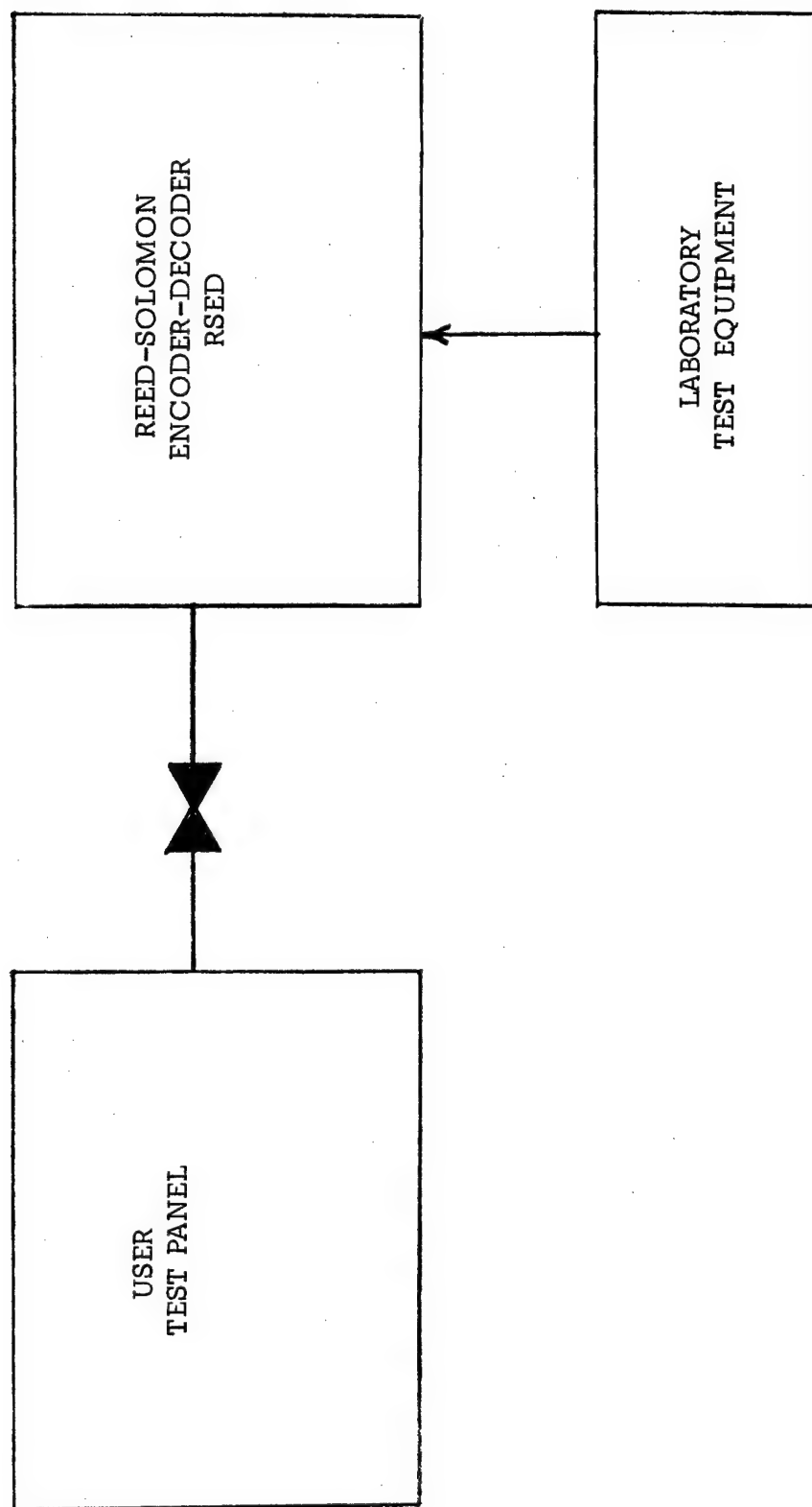
2.0 DECODER

2.1 Errata Correction Capability

The RSED module has the capability to reconstruct the original information bits when the received characters of above encoded words are within the errata correction capabilities of the Reed-Solomon code are given in Table 1. The module will correct all standard (31,15) and short (16,4) encoded words with errors and erasures inserted up to and including the maximum capability.

2.2 Message Throughput Rate

The RSED module will decode a message of 109 (5 bits plus erasure bit) characters consisting of one (16,4) and three (31,15) code words at the rate of 128 messages per second.



RSED BLOCK DIAGRAM

Figure 1

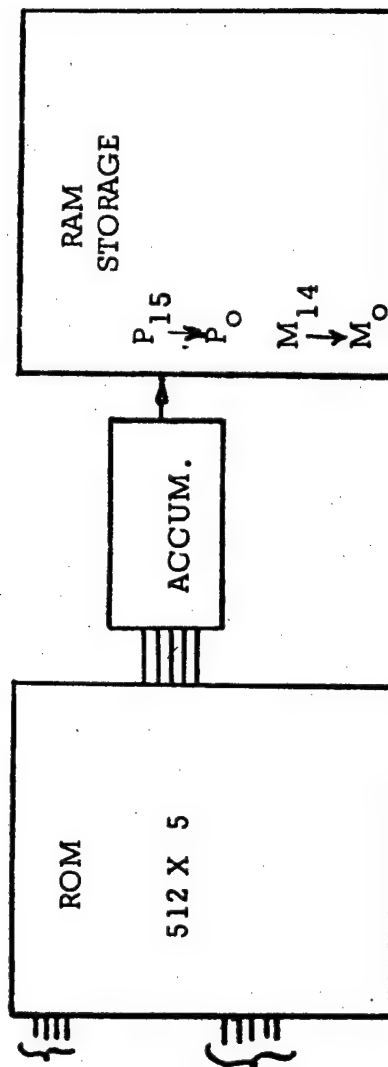
$$\begin{aligned}
 P_{15} &= h_0 M_{14} \oplus h_1 M_{13} \dots \oplus h_{14} M_0 \\
 P_{14} &= h_0 M_{13} \oplus h_1 M_{12} \dots \oplus h_{14} P_{15} \\
 P_{13} &= h_0 M_{12} \oplus h_2 M_{11} \dots \oplus h_{14} P_{14} \\
 P_0 &= h_0 P_{15} \oplus h_1 P_{14} \dots \oplus h_{14} P_1
 \end{aligned}$$

Constants

$h_0 \rightarrow h_{14}$

Variables

M = DATA CHARACTERS
 P = PARITY CHARACTERS



ENCODING ALGORITHM

Figure 2

2.3 Maximum Decoder Delay

The maximum time to decode a standard message consisting of 1 Header plus 3 long words shall be consistent with the required throughput. Specifically, the average delay must be less than 7.8125 msec. For certain applications the maximum permissible delay is ≈ 6.7 msec, and the decoder delay vs. errata profiles and related probabilities will be measured to determine what percentage of time does the decoder exceed 6.7 msec. A message loss rate of 1 message in 10^4 messages is acceptable.

2.4 Decoder Failure

When the number of errata exceeds the decoding capability of the Reed-Solomon code the decoding algorithm will detect this condition. The RSED module will generate a decoding failure condition in this event. The module will always generate a failure when the number of declared erasures exceed 16, for the (31,15) code and 12 for the (16,4) code.

3.0 ROUND TRIP TIMING (RTT)

3.1 RTT Decode

The RSED module will accept a (16,4) Reed-Solomon code word and determine if it is an RTT interrogation matching a specific stored reference. The reference is a 20 bit message encoded into a (16,4) codeword. It shall correctly recognize the code word containing errata up to the maximum capability of the (16,4) code shown in Table 1.

The RTT decode time shall not exceed 75 usec measured from the receipt of the last character in the code word.

3.2 RTT Turn Around Time

For a RTT interrogation message matching the stored reference the module will generate a recognition signal and accept a twenty bit reply message for encoding in a (16,4) code word. The time to complete the recognition and encoding shall not exceed 375 usec measured from the receipt of the last character of the RTT interrogation message.

III. RSED TEST PLAN

1.0 Encoder Test

1.1 Encoder Accuracy Test

This test will be conducted on a message basis to verify the correctness of the encoding process. A large class of code words with variable data characters for the (31,15) and (16,4) codes will be presented to the RSED via the User Test Panel and the encoder output will be compared with the correct output presented in the test data sheets.

The encoding algorithm is shown in block form in Figure 2.

Number of Errors	Maximum Number of Erasures		
	(31,15)	(16,4)	
0	> 16	> 12	Decoder Failure
0	16	12	
1	14	10	
2	12	8	
3	10	6	
4	8	4	
5	6	2	
6	4	0	
7	2	---	
8	0	---	
> 8	---	---	Decoder Failure

Table 1. ERRATA CORRECTION CAPABILITY OF THE REED-SOLOMON CODES

1.2 Encoder Timing Test

This test will be conducted using message blocks consisting of one (16,4) and three (31,15) code words. Each code word of the message block will be timed using front panel test points with standard laboratory test equipment and shall not exceed 300 microseconds for the respective code word.

2.0 Decoder Tests

2.1 Decoder Accuracy Test

This test will be conducted on a message block basis to verify the decoding process. A set of test words containing the number of errors and erasures shown in Table 2 will be prepared and presented in the test data sheets. The decoded word is compared with the transmitted word and the results of this comparison shall be noted on the test data sheet. A quality word shall be displayed on the User Test Panel for each code word which indicates "A Cannot Decode Code Word" and also displays the number of errors.

2.2 Decoder Timing Test - Single Word

This test will determine the decoding time of the code words as a function of the number of errata (errors and erasures) and their location in the words. The objective will be to find the worst case decoding time and determine those errata cases to be used in the message decoding timing tests.

2.2.1 Worst Case Decoding Time

The candidates for the worst case decoding times are shown in Table 3. It is expected that the worst cases are 8 errors and 6 errors for the (31,15) and (16,4) codes respectively. The time to decode these words will be determined. The parameters of number of errata and locations will be varied to determine the trend of decoding times and the worst case established.

2.2.2 Decoding Time Profile

Using the worst case errata locations the decoding time as a function of errata will be determined. This test will identify those errata cases which might cause the RSED message decoding time to exceed the message throughput rate and maximum decoding delay specifications. The timing profile will be used to estimate message decoding times and then messages, consisting of one (16,4) code word and three (31,15) code words will be prepared and presented to the RSED hardware.

Number of Errors	Number of Erasures (31,15) (16,4)	Number of Erasures (31,15) only
0	0, 4, 8, 12,	13, 16
1	0, 3, 6, 10,	12, 14
2	0, 1, 5, 8,	11, 12
3	0, 3, 5, 6,	7, 10
4	0, 2, 3, 4,	6, 8,
5	0, 1, 2,	4, 6,
6	0	1, 2, 4,
7	-----	0, 1, 2,
8	-----	-----

Table 2. DECODER ACCURACY TEST CASES

Number of Errata		Position of Errata
Errors	Erasures (31,15), (16,4) (31,15) only	
8	----	0
0	12	16
3	6	10
4	4	8
5	2	6
6	0	4
7	---	2
		Errors in last 3 parity characters, other errors in information characters.
		All erasures concentrated in information characters.
		Errors in last 3 parity characters all other errata in information characters.

Table 3. WORST CASE DECODING TIME CANDIDATE

2.3 Decoder Timing Test - Messages

The time to decode messages as a function of errata content, using a distribution of errata and also worst case errata location, will be determined. If the worst case message decoding times exceed the specifications of message throughput or maximum decoding delay then a statistical analysis will be used to determine the probability of message loss due to excess decoding time.

2.4 Decoder Failure Test

Using the same procedure as in the decode accuracy test, Sec. 2.1 code words whose errata content exceeds the code capability shown in Table 1 will be presented to the RSED. It will be demonstrated that if the number of erasures exceeds 16 or 12 for the (31,15) and (16,4) codes respectively the RSED module will generate a decoding failure. The performance of the RSED for errata patterns that exceed the code capability will be investigated. It is noted that the decoding algorithm does not guarantee any performance in this event.

3.0 Round Trip Timing (RTT) Message Processing Tests

3.1 RTT Message Recognition Accuracy

RTT messages, (16,4) code words, will be presented to RSED module for processing. It will be demonstrated that message addressed to the terminal will be recognized correctly when errata is inserted up to the correction capability of the (16,4) code shown in Table 1. The cases to be tested will be those shown in Table 2 for the (16,4) code. It will also be demonstrated that messages not addressed to the terminal will be rejected by the RTT recognition process. In this case the twenty bit address message of the terminal will be encoded with one of the twenty bits changed. The resulting (16,4) code word will be presented to the RSED module for RTT processing with the same previously tested errata combinations.

3.2 RTT Recognition Processing Time

This test will determine the time required to successfully recognize an RTT message addressed to the terminal. This time will be measured from the receipt of the last of the sixteen code word characters to the generation of the RTT recognition flag. A set of correct messages with errata inserted, as in Table 2, in various positions will be presented to the RSED module. Standard Laboratory test shall be used to measure the RTT Recognition Processing time. These times will not exceed 0.075 msec.

3.3 Total RTT Turnaround Time

This test will measure the time required to recognize an RTT message addressed to the terminal and subsequently encode a (16,4) code word reply. This time will be measured from the receipt of the last code character until the last encoded character is presented at the RSED encoder output. It is assumed that since every time slot is a possible RTT interrogation that the RTT reply will be prepared for each time slot and is immediately available at the Encoder input when the RTT recognition flag is generated by the RSED module. The set of messages used in 3.1 will be presented to the module and a test message presented to the encoder when the recognition flag is generated. Timing measurements will be made to verify that the total RTT turnaround time does not exceed 375 microseconds.

4.0 Multifunction RSED Tests

This series of tests will demonstrate the RSED module is capable of performing combinations of encode/decode/RTT (as specified by the SOW) as described below.

4.1 Decode Slot "n" - Encode Slot "n + 1"

This test will demonstrate that the RSED module is capable of decoding a standard message consisting of 1 Header plus 3 Standard Words in time slot "n," to be followed by encode of 1 Header plus 3 Standard Words for transmission in slot n + 1.

It will be shown that the encoding can be performed while the decoding process is continuing. Both decode and encode operation will be within specified timing limits during this test.

4.2 Decode Slot "n" - RTT Decode/Encode Slot "n"

This test will demonstrate that the RSED module is capable of decoding a standard message consisting of 1 Header plus 3 Standard Words in time slot "n" and at the same time (during time slot "n") process a RTT Decode/Encode without interrupting the ongoing decode process. Both the decode and the RTT Decode/Encode will be performed with specified timing limits during this test.

4.3 RTT Decode/Encode Slot "n" - Encode Slot "n + 1"

This test will demonstrate that the RSED module is capable of processing a RTT Decode/Encode in slot "n" and is able to then encode a short message consisting of 1 Header (e.g. RTT interrogation) or a Standard Message consisting of 1 Header plus 3 Standard Words, in slot "n + 1".

IV. TEST RESULTS SUMMARY

In addition to the test data taken during the RSED Acceptance Test a summary of the test results will be prepared. This document will summarize the results of each test and include a comparison between system requirements and actual performance.